1/3.2-Inch 2-Megapixel CMOS Digital Image Sensor

Part number: MT9D011W00STC
MT9D011D00STC

For the lastest data sheet revision, please refer to Aptina's Web site: www.aptina.com

Features

- DigitalClarity™ CMOS Imaging Technology
- High frame rate
- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Support for long integration times
- 2 x 2 binning
- Anti-aliasing function
- Anti-eclipse function
- Operating modes: snapshot and flash control, high frame rate preview, electronic panning
- Programmable controls: gain, frame size/rate, exposure, left-right and top-bottom image reversal, window size, panning, zoom and decimation
- 10-bit analog-to-digital converter (ADC) with three external inputs
- Support for external mechanical shutter
- Internal master clock generated from on-chip phase locked loop (PLL)
- Electronic rolling shutter (ERS)

Applications

- Cellular phones
- PC cameras
- PDAs
- Toys and other battery-powered products

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical Format		1/3.2-inch (4:3)
Active Imager Size		4.48mm(H) x 3.36mm(V), 5.60mm Diagonal
Active Pixels		1,600H x 1,200V
Pixel Size		2.8µm x 2.8µm
Color Filter Array		RGB Bayer Pattern
Shutter Type		Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		40 MPS/40 MHz
Frame Rate	UXGA (full frame, 1,600H x 1,200V)	15 fps at 36 MHz
	SVGA (preview, 800H x 600V)	30 fps at 36 MHz
ADC Resolution		10-bit, on-chip
Responsivity		1.0 V/lux-sec (550nm)
Dynamic Range		71.5dB
SNR_{MAX}		42.3dB
Supply Voltage	I/O Digital	1.7V–3.1V
	Core Digital	1.7V–1.9V (1.8V nominal)
	Analog	2.5V–3.1V (2.8V nominal)
Power Consumption		77mW at 30 fps, 36 MHz, Preview mode
		125mW at 15 fps, (V_{AA}, VAAPIX and V_{DD} only) 36 MHz, Full frame mode
Operating Temperature		-30°C to +70°C
Packaging		Wafer or die

Note:Typical operating power does not include the I/O power or the PLL.

Table 2: Available Part Numbers

Part Number	Description
Wafer	MT9D001W00STC
Die	MT9D001D00STC

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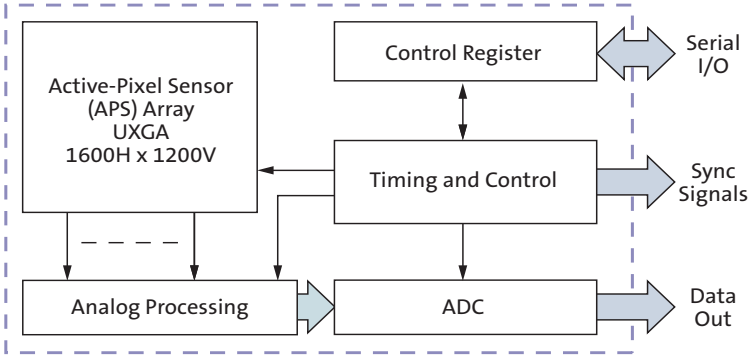
General Description

The Aptina® MT9D011 is an oversize UXGA-format CMOS active-pixel digital image sensor with a pixel array of 1632H x 1216V. It incorporates sophisticated on-chip camera functions such as windowing, mirroring, row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and achieves very low power consumption.

The 2-megapixel CMOS image sensor features DigitalClarity—Aptina's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

When operated in default mode, the sensor generates a UXGA image at 15 frames per second (fps). An on-chip ADC generates a 10-bit value for each pixel. The pixel data is output on a 10-bit output bus and qualified by an output data clock (PIXCLK), together with LINE_VALID and FRAME_VALID signals. A FLASH output strobe is provided to allow an external Xenon or LED light source to synchronize with the sensor exposure time. The sensor can be programmed by the user to control the frame size, exposure, gain setting, and other parameters.

Figure 1: Block Diagram



Introduction

The MT9D011 is a progressive-scan sensor that generates a stream of pixel data qualified by LINE_VALID and FRAME_VALID signals. An on-chip PLL generates the master clock from an input clock of 4 MHz to 40 MHz. In default mode, the data rate (pixel clock) is the same as the master clock frequency, which means that one pixel is generated every master clock cycle. The sensor block diagram is shown in Figure 1.

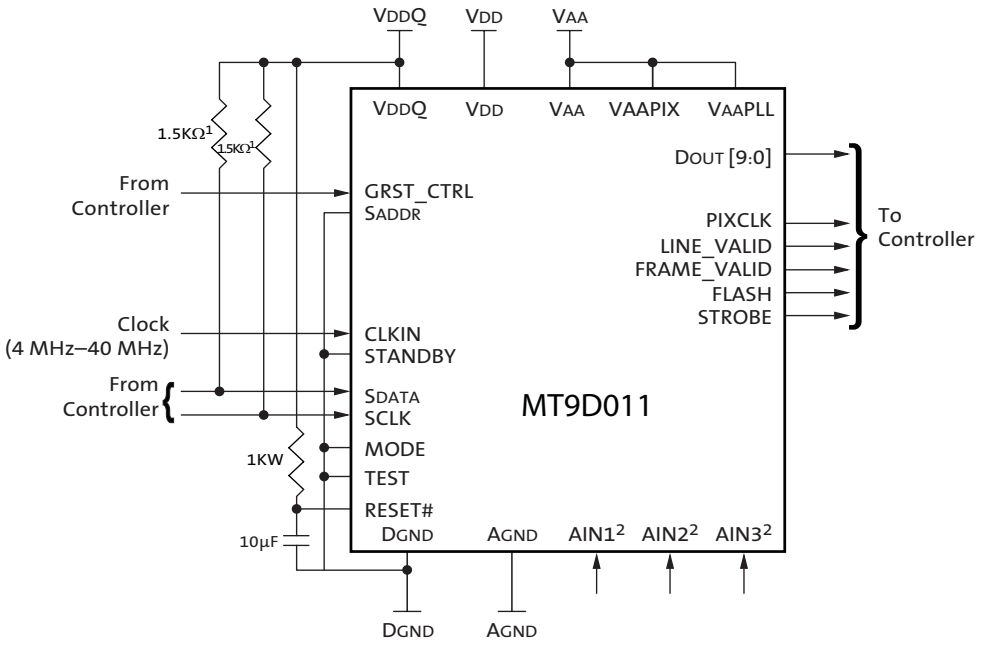
The core of the sensor is an active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row. In the time interval between resetting a row and reading that row, the pixels in that row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. After a row is read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 10-bit value for each pixel in the array. The pixel array contains optically active and light-shielded "black" pixels. The black pixels are used to provide data for on-chip offset correction algorithms ("black level" control).

The sensor contains a set of 16-bit control and status registers that can be used to control many aspects of the sensor operations. These registers can be accessed through a two-wire serial interface. In this document, registers are specified either by name (e.g., column start) or by register address (e.g., Reg0x04). Fields within a register are specified by bit or by bit range (e.g., Reg0x20[0] or Reg0x0B[13:0]). The control and status registers are described in "1 = always 1 0 = always 0 d = programmable ? = read-only (R/O) R/W = Read/Write" on page 18.

The output from the sensor is a Bayer pattern: alternate rows are a sequence of either green/red pixels or blue/green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

The sensor generates a UXGA-sized image by default, with 10 parallel data outputs per pixel, and separate LINE_VALID, FRAME_VALID, and pixel clock outputs. All timing control is performed on-chip.

Figure 2: Typical Configuration (Connection)



Note: 1. Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.
2. If not used, leave unconnected.

Table 3: Signal Description

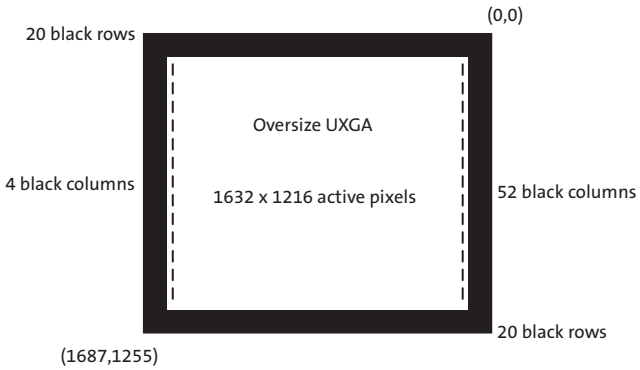
Name	Type	Description
RESET#	Input	Asynchronous active-low reset. When asserted, data output stops and all internal registers are restored to their factory default settings.
AIN1	Input	Analog input port. If enabled by Reg0xE3, the pin is sampled once per row by the on-chip analog-to-digital converter (ADC).
AIN2	Input	Similar to AIN1.
AIN3	Input	Similar to AIN1.
SCLK	Input	Serial clock for access to control and status registers.
SADDR	Input	Selects the device address for the serial interface. See "Slave Address" on page 15.
STANDBY	Input	Multifunction pin to control device addressing, power-down, and pin tri-state functions. When LOW, the sensor functions normally. When HIGH, the sensor may enter a low power state and may put certain outputs in a High-Z. See "Power-Saving Modes" on page 37, "By applying maximum analog and digital gain, it is possible to achieve a total gain of 128. It is not recommended to operate the sensor with such high gain since this may introduce visible noise in the image. Digital gain should therefore be limited to a factor of 2 in order to keep the total gain below 32x." on page 37, and "Slave Address" on page 15.
CLKIN	Input	Input clock to PLL or master clock.
TEST	Input	Enable manufacturing test modes. Wire to DGND for functional operation.
MODE	Input	Tie to DGND for normal operation.
GRST_CTR	Input	Controls the global reset operation.
SDATA	I/O	Serial data for reads from and writes to control and status registers.
DOUT9	Output	Pixel data output 9 (most significant bit (MSB)).
DOUT8	Output	Pixel data output 8.
DOUT7	Output	Pixel data output 7.
DOUT6	Output	Pixel data output 6.
DOUT5	Output	Pixel data output 5.
DOUT4	Output	Pixel data output 4.
DOUT3	Output	Pixel data output 3.
DOUT2	Output	Pixel data output 2.
DOUT1	Output	Pixel data output 1.
DOUT0	Output	Pixel data output 0 (least significant bit (LSB)).
LINE_VALID	Output	LINE_VALID. Asserted during a line of valid pixel data. (The operation of this signal can be controlled by Reg0x25[15:14].)
FRAME_VALID	Output	FRAME_VALID. Asserted during a frame of valid pixel data.
PIXCLK	Output	Pixel clock. By default, pixel data, LINE_VALID, and FRAME_VALID are valid on the rising edge of this clock. This signal can be inverted and delayed under the control of Reg0x0A.
STROBE	Output	Synchronization pulse for mechanical shutter in global reset mode.
FLASH	Output	Synchronization pulse for external light source.
VDDQ	Power	I/O power.
VDD	Power	Digital power.
DGND	Power	Digital and I/O ground.
VAAPLL	Power	PLL power.
VAA	Power	Analog power.
AGND	Power	Analog ground.
VAAPIX	Power	Analog power for pixel array.

Pixel Array Structure

The MT9D011 pixel array is configured as 1688 columns by 1256 rows (shown in Figure 3). The first 52 columns and the first and the last 20 rows of pixels are optically black and are used for the automatic black level adjustment. The last four columns are also optically black.

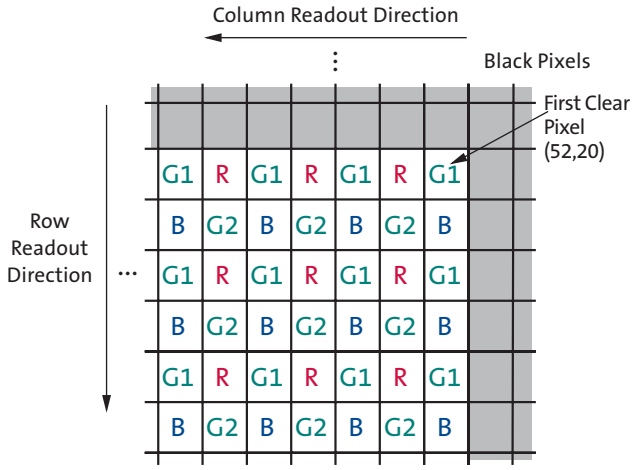
The optically active pixels are used as follows: In default mode a UXGA image (1600 columns by 1200 rows) is generated, starting at row 28, column 60. A four-pixel boundary of active pixels can be enabled around the image to avoid boundary effects during color interpolation and correction. During mirrored readout, the region of active pixels used to generate the image is offset by one pixel in each mirrored direction so that the readout always starts on the same color pixel.

Figure 3: Pixel Array



The MT9D011 uses a Bayer color pattern as shown in Figure 4. The even-numbered rows contain green and red color pixels; odd-numbered rows contain blue and green color pixels. Even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels. The color order is preserved during mirrored readout.

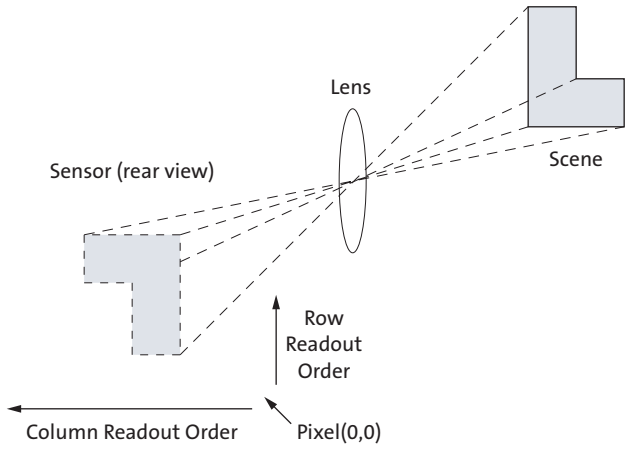
Figure 4: Pixel Color Pattern Detail (Top Right Corner)



Default Readout Order

By convention, the MT9D011 pixel array is shown with pixel (0,0) in the top right-hand corner (see Figure 4). This reflects the actual layout of the array on the die. When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 5. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 3. By convention, data from the sensor is shown with the first pixel read out—pixel (52,20) in the case of the MT9D011—in the top left-hand corner. See Figure 6.

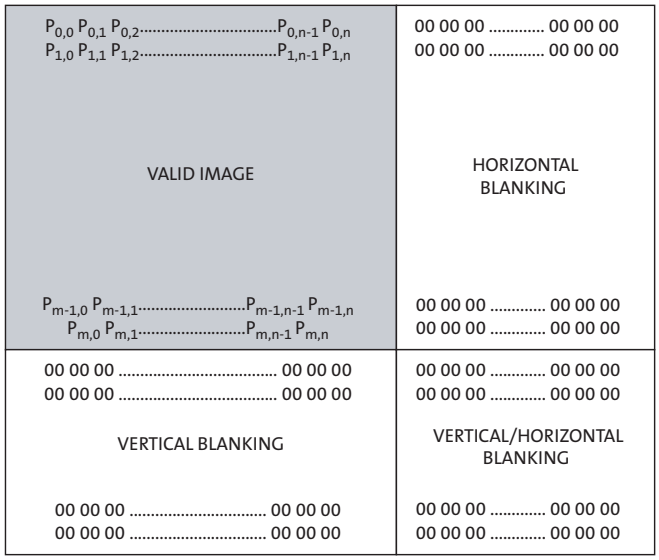
Figure 5: Imaging a Scene



Output Data Format

MT9D011 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking as shown in Figure 6. The amount of horizontal and vertical blanking is programmable. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in the next section.

Figure 6: Spatial Illustration of Image Readout



Output Data Timing

MT9D011 output data is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one pixel datum is output on the 10-bit DOUT output every PIXCLK period. By default, the PIXCLK signal runs at the same frequency as the master clock, and its rising edges occur one-half of a master clock period after transitions on LINE_VALID, FRAME_VALID, and DOUT (see Figure 7). This allows PIXCLK to be used as a clock to sample the data. PIXCLK is continuously enabled, even during the blanking period. The MT9D011 can be programmed to delay the PIXCLK edge relative to the DOUT transitions from 0 to 3.5 master clocks, in steps of one-half of a master clock. This can be achieved by programming the corresponding bits in Reg0x0A. The parameters P, A, and Q in Figure 8 are defined in Table 4 on page 13.

Figure 7: Pixel Data Timing Example

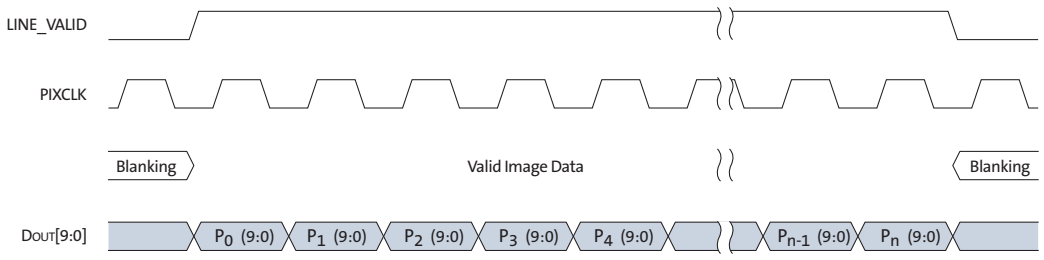
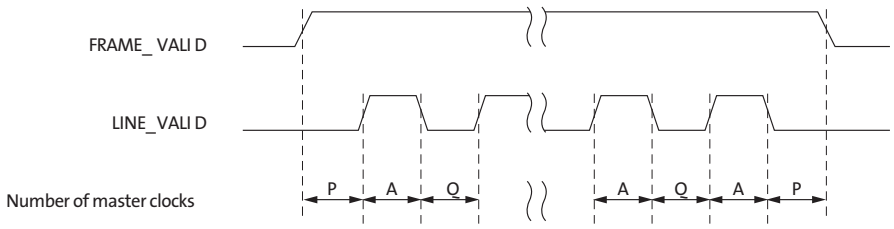


Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals



The sensor timing (Table 4) is shown in terms of pixel-clock and master-clock cycles (see Figure 7 on page 11). The recommended master clock frequency is 36 MHz. Increasing the integration time to more than one frame will cause the frame time to be extended. The equations in Table 4 assume integration time is less than the number of rows in a frame (Reg0x09 < Reg0x03/S + BORDER + VBLANK_REG). If this is not the case, the number of integration rows must be used instead to determine the frame time as shown in Table 5.

Table 4: Frame Time

Parameter	Name	Equation	Default Timing at 36 MHz, Dual ADC Modes
HBLANK_REG	Horizontal Blanking Register	Reg0x07 if Reg0xF2[0] = 0 Reg0x05 if Reg0xF2[0] = 1	0x15C = 348 pixels
VBLANK_REG	Vertical Blanking Register	Reg0x8 if Reg0xF2[1] = 0 Reg0x6 if Reg0xF2[1] = 1	0x20 = 32 rows
ADC_MODE	ADC mode	Reg0xF2[3] = 0: Reg0x20[10] Reg0xF2[3] = 1: Reg0x21[10]	
PIXCLK_PERIOD	Pixel clock period	ADC_MODE = 0: Reg0x0A[2:0] ADC_MODE = 1: Reg0x0A[2:0]*2	1 ADC_MODE: 55.556ns 2 ADC_MODE: 27.778ns
S	Skip Factor	For skip 2x mode: S = 2 For skip 4x mode: S = 4 For skip 8x mode: S = 8 For skip 16x mode: S = 16 otherwise, S = 1	1
A	Active Data Time	(Reg0x04/S) * PIXCLK_PERIOD	1,600 pixel clocks = 1,600 master = 44.44µs
P	Frame Start/End Blanking	6 * PIXCLK_PERIOD (can be controlled by Reg0x1F)	6 pixel clocks = 12 master = 0.166µs
Q	Horizontal Blanking	HBLANK_REG * PIXCLK_PERIOD	348 pixel clocks = 348 master = 9.667µs
A + Q	RowTime	((Reg0x04/S) + HBLANK_REG) * PIXCLK_PERIOD	1,948 pixel clocks = 1,948 master = 54.112µs
V	Vertical Blanking	VBLANK_REG * (A + Q) + (Q - 2*P)	62,672 pixel clocks = 62,672 master = 1.741ms
Nrows * (A+Q)	Frame Valid Time	(Reg0x03/S + BORDER) * (A + Q) - (Q - 2*P)	2,337,264 pixel clocks = 2,337,264 master = 64.925ms
F	Total Frame Time	(Reg0x03/S) + BORDER + VBLANK_REG) * (A + Q)	2,399,936 pixel clocks = 2,399,936 master = 66.665ms

Notes: 1. Skip factor should be multiplied by 2 if binning is enabled.

Table 5: Frame—Long Integration Time

Parameter	Name	Equation (master clock)
V'	Vertical Blanking (long integration time)	(Reg0x09 - (Reg0x03)/S + BORDER)) * (A + Q) + (Q - 2*P)
F'	Total Frame Time (long integration time)	(Reg0x09)*(A + Q)

Two-wire Serial Register Interface

This section describes the two-wire serial interface bus that can be used in any functional sensor mode.

The two-wire serial interface bus enables R/W access to control and status registers within the MT9D011.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and used to synchronize transfers. The master is responsible for driving a valid logic level on SCLK at all times. Data is transferred between the master and the slave on a bi-directional signal (SDATA). The SDATA signal is pulled up to VDD off-chip by a 1.5kΩ resistor. Either the slave or master device can drive the SDATA line low—the interface protocol determines which device is allowed to drive the SDATA line at any given time.

Protocol

The two-wire serial interface bus defines the transmission codes as follows:

- a start bit
- the slave device 8-bit address
- a(an) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence is executed as follows:

1. The master sends a start bit.
2. The master sends the 8-bit slave device address. The last bit of the address determines if the request is a read or a write, where a “0” indicates a write and a “1” indicates a read.
3. The slave device acknowledges receipt of the address by sending an acknowledge bit to the master.
4. If the request is a write, the master then transfers the 8-bit register address, indicating where the write takes place.
5. The slave sends an acknowledge bit, indicating that the register address has been received.
6. The master then transfers the data, eight bits at a time, with the slave sending an acknowledge bit after each eight bits.

The MT9D011 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows.

1. The master sends the write-mode slave address and 8-bit register address, just as in the write request.
2. The master then sends a start bit and the read-mode slave address, and clocks out the register data, eight bits at a time.
3. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred.

4. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are high. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW data line transition while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH data line transition while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and one bit of direction. A "0" in the LSB (least significant bit) of the address indicates write mode, and a "1" indicates read mode. The default slave addresses used by the MT9D011 are 0xBA (write address) and 0xBB (read address). Reg0x0D[10] or the SADDR pin can be used to select the alternate slave addresses 0x90 (write address) and 0x91 (read address).

Writes to Reg0x0D[10] are inhibited when the standby pin is asserted (all other writes proceed normally). This allows two sensors to co-exist as slaves on this interface, but they must be addressed independently. Enable this capability as follows:

After RESET, both sensors use the default slave address. Reads or writes on the serial register interface to the default slave address are decoded by both sensors simultaneously.

1. After RESET, assert the STANDBY signal to one sensor and negate the STANDBY signal to the other sensor.
2. Perform a write to Reg0x0D with bit 10 set. The sensor with STANDBY asserted ignores the write to bit 10 and continues to decode at the default slave address.

The sensor with STANDBY negated has its Reg0x0D[10] set and responds to the alternate slave address for all subsequent read and write operations, as shown in See Table 6.

Table 6: Slave Address Options

SADDR Pin	Reg0xD[10]	Slave Address	
		Write	Read
0	0	0x090	0x091
0	1	0x0BA	0x0BB
1	0	0x0BA	0x0BB
1	1	0x090	0x091

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the high period of the two-wire serial interface clock—it can only change when the serial clock is low. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-Acknowledge Bit

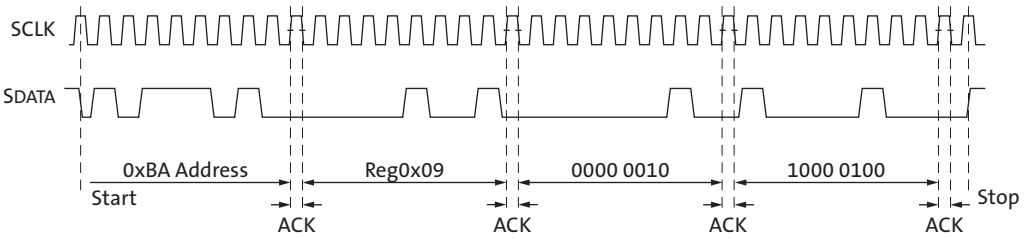
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 9. A start bit given by the master starts the sequence, followed by the write address. The image sensor then sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

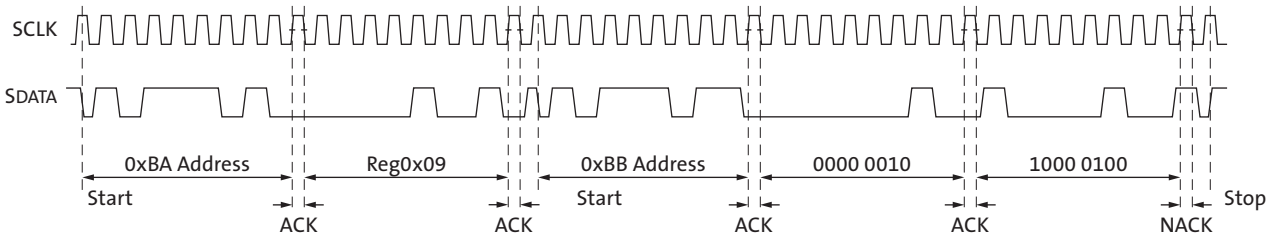
Figure 9: WRITE Timing to R0x09:0—Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 10. First the master writes the register address, as in a write sequence. Then a start bit and the read address specify that a read is about to happen from the register. The master clocks out the register data, eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

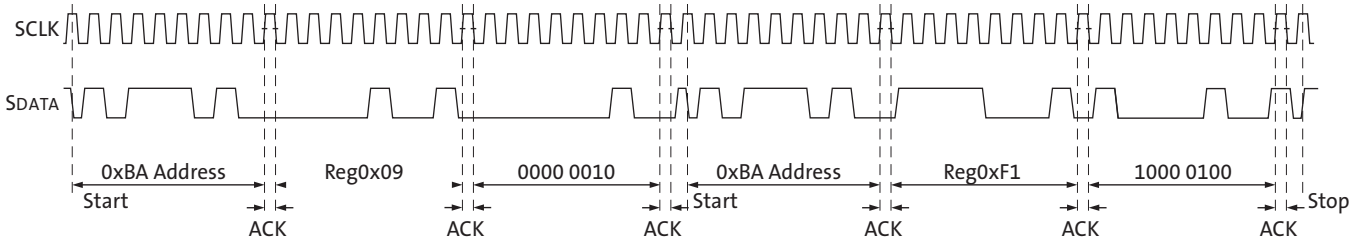
Figure 10: READ Timing from R0x09:0; Returned Value 0x0284



8-Bit Write Sequence

To be able to write one byte at a time to the register, a special register address is added. The 8-bit write is done by writing the upper 8 bits to the desired register, then writing the lower 8 bits to the special register address (Reg0xF1). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register. In Figure 11, a typical sequence for 8-bit writes is shown. The second byte is written to the special register (Reg0xF1).

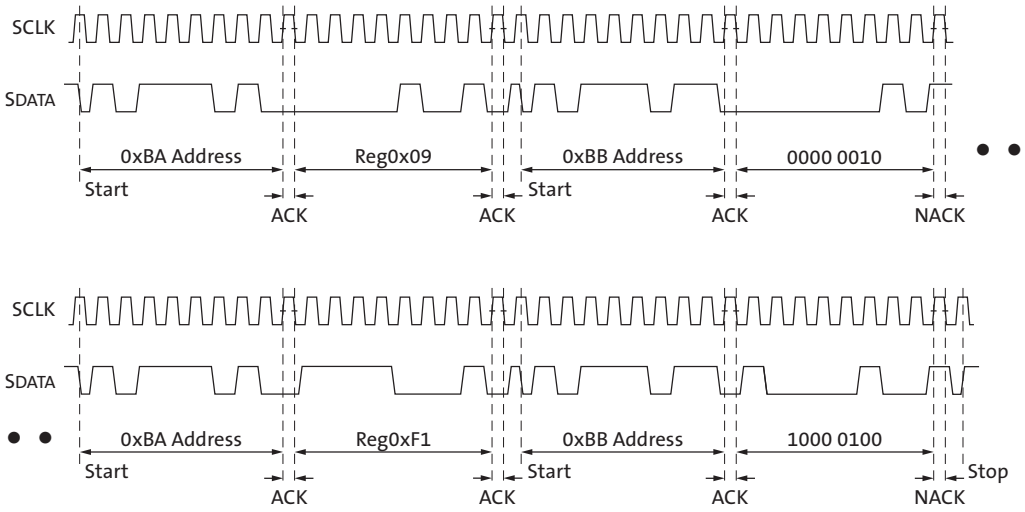
Figure 11: WRITE Timing to R0x09:0—Value 0x0284



8-Bit Read Sequence

To read one byte at a time, the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (Reg0xF1), the lower 8 bits are accessed (Figure 12). The master sets the no-acknowledge bits shown.

Figure 12: READ Timing from Reg0x09; Returned Value 0x0284



Note: 1 = always 1
0 = always 0
d = programmable
? = read-only (R/O)
R/W = Read/Write

Feature Description

PLL Generated Master Clock

The MT9D011 has an on-chip PLL that can generate a master clock in the range of 36 MHz to 40 MHz from an input reference clock of 4 MHz to 40 MHz. It is possible to bypass the PLL and use CLKIN as master clock. This is controlled by Reg0x65[15]. When the PLL is bypassed (Reg0x65[15] = 1), it is recommended to set the PLL in power down mode by setting Reg0x65[14] = 1. Default mode is PLL bypassed and in powerdown mode.

Reg0x66 and Reg0x67 controls the frequency setting of the generated clock.

PLL Settings

The PLL is controlled through its M, N and P parameters, as set in registers 0x66 and 0x67. The PLL output frequency (fout) has the following relationship to the input frequency (fin):

$$fout = fin*M/(2*(N+1)*(P+1))$$

Not all possible settings are allowed. M must be 16 or higher. Also, the following restrictions on frequencies must be obeyed:

Frequency	Equation	Min [MHz]	Max [MHz]
fPFD	fin/(N+1)	2	16
fVCO	fPFD*M	110	220
fout	fVCO/(2*(P+1)	36	40

PLL Power-up

The PLL takes time to power up. During this time, the behavior of its output clock is not guaranteed. The PLL is in power-down by default and must be turned on manually. When using the PLL, the correct power-up sequence after chip reset is as follows:

1. Program PLL frequency settings (Reg0x66 and Reg0x67)
2. Power up PLL (Reg0x65[14] = 0)
3. Wait for PLL settling time > 150µs
4. Turn off PLL bypass (Reg0x65[15] = 0)

Window Control

Window Start

The row and column start address of the displayed image can be set by Reg0x01 (Row Start) and Reg0x02 (Column Start).

Window Size

The size of the displayed image can be set by Row Width Reg0x03 and Column Width Reg0x04. The default image size is 1600 columns and 1200 rows (UXGA).

The window start and size registers can be used to configure an image size between 17 and 1632 columns and between 2 and 1216 rows.

Pixel Border

When Reg0x20[9:8] are both set, a four pixel border is added around the specified image. This border can be used as extra pixels for image processing algorithms. The border is independent of the readout mode, which means that even in skip, zoom, and binning modes, a four pixel border is output in the image. When enabled, the row and column widths are eight pixels larger than the values programmed in Reg0x03 and Reg0x04. If the border is enabled but not shown in the image (Rex0x20[9:8] = 01), the horizontal blanking and vertical blanking values are eight pixels larger than the values programmed in the blanking registers.

Readout Modes

Readout Speeds and Power Savings

The MT9D011 has two ADCs to convert the pixel values to digital data. Because the ADCs run at half the master clock frequency, it is possible to achieve a data rate equal to the master clock frequency. By turning off one of the ADCs, the power consumption of the sensor is reduced. The pixel clock is then reduced by a factor of two.

In Reg0x20 or Reg0x21, bit 10 chooses between the two modes:

0: Use both ADCs and read out at the set pixel clock frequency (Reg0x0A, bits 3:0).

1: Use 1 ADC and read out at half the set pixel clock frequency (Reg0x0A, bits 3:0).

This can be used, for instance, when the camera is in preview mode. To make the transitions between two sensor settings easier, some simple context switching is described in "Context Switching" on page 28.

Column Mirror Image

By setting Reg0x20[1] = 1, the readout order of the columns are reversed as shown in Figure 13. The starting color is preserved when mirroring the columns.

Row Mirror Image

By setting Reg0x20[0] = 1 Reg0x21 in Context A, the readout order of the rows are reversed as shown in Figure 14. The starting color is preserved when mirroring the rows.

Figure 13: Six Pixels in Normal and Column Mirror Readout Modes

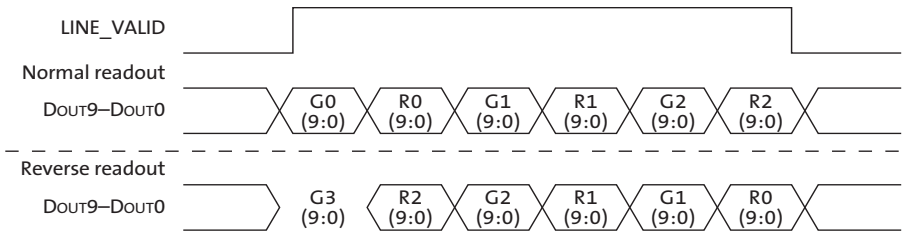
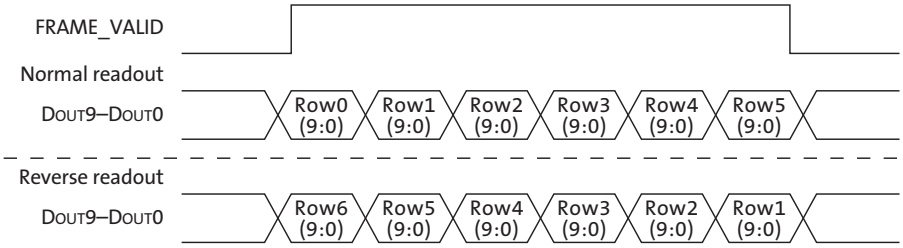


Figure 14: Six Rows in Normal and Row Mirror Readout Modes



Column and Row Skip

This section assumes Context B. If Context A is used, replace all references to Reg0x20 with Reg0x21.

By setting Reg0x20[4] = 1 or Reg0x20[7] = 1, skip is enabled for rows or columns, respectively. When skip is enabled, the image is subsampled. The amount of skipping is set by Reg0x20[3:2] (rows) and Reg0x20[6:5] (columns) according to Table 7.

Table 7: Skip Values

Bit values	Skip Value
00	2
01	4
10	8
11	16

The number of rows or columns read out is what is set in Reg0x03 or Reg0x04, respectively, divided by the Skip Value in this table.

In all cases, the row and column sequencing ensures that the Bayer pattern is preserved.

Column skip examples are shown in Figures 15 through 18.

Figure 15: Eight Pixels in Normal and Column Skip 2x Readout Modes

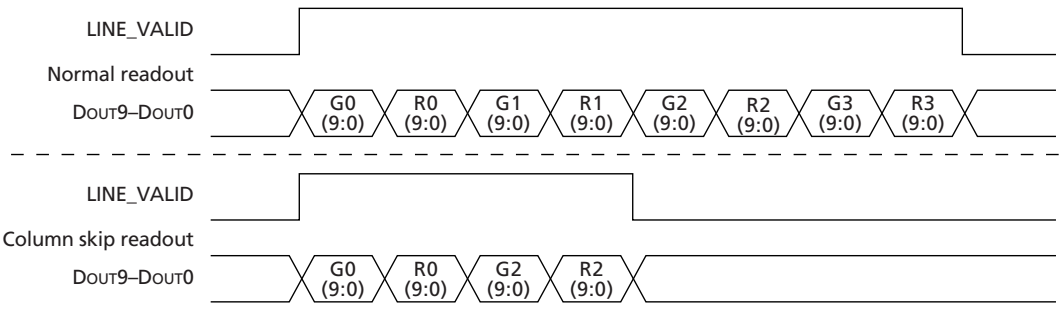


Figure 16: Sixteen Pixels in Normal and Column Skip 4x Readout Modes

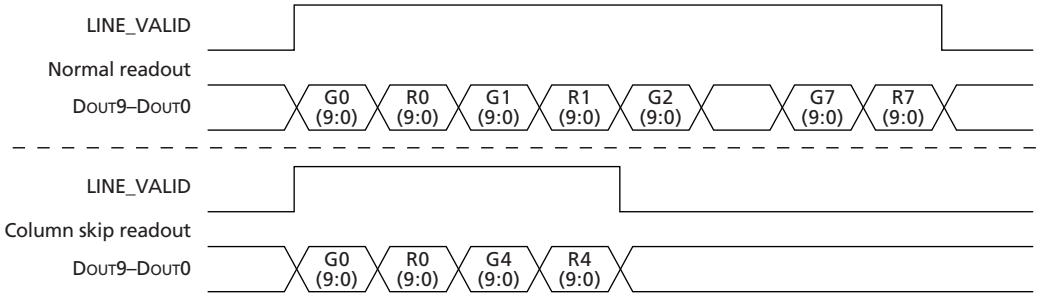


Figure 17: Thirty-two Pixels in Normal and Column Skip 8x Readout Modes

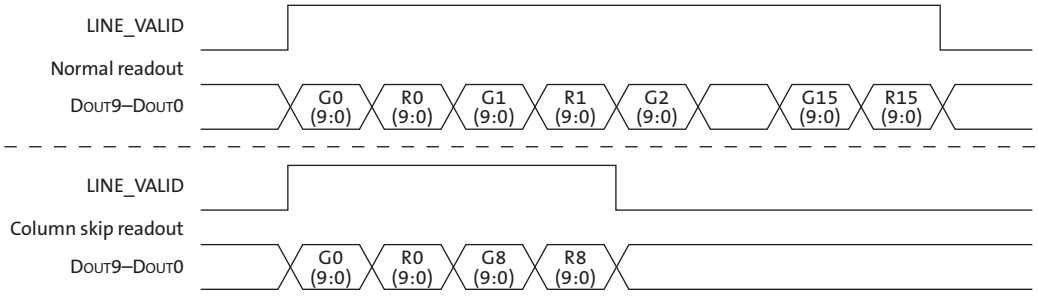
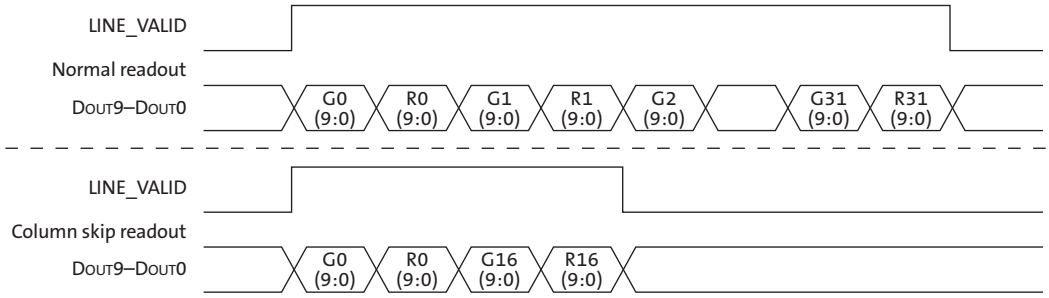


Figure 18: Sixty-four Pixels in Normal and Column Skip 16x Readout Modes



Digital Zoom

Reg0x20[13] enables a digital zoom of 2x to 16x to be applied. The zoom value is set in Reg0x20[12:11] according to Table 8.

In zoom mode, the pixel data rate is slowed by the zoom factor, and a number of additional blank rows are added between output rows (see Table 8). This is designed to give the controller logic the necessary time to repeat data, filling in a larger window with repeated data.

Table 8: Zoom Values

Bit values	Zoom Value	Blank Rows
00	2	1
01	4	3
10	8	7
11	16	15

The pixel clock speed is not affected by this operation, therefore the output data for each pixel is valid for zoom factor number of pixel clocks. Every row is followed by a number of blank rows (with their own LINE_VALID, but all data bits = 0) of equal time.

In zoom modes, Reg0x03 and Reg0x04 still specifies the window size out of the sensor including the extra blanking, so the active image read out is, in effect, smaller than the output image.

Figures 19 through 23 show the data coming from the sensor in the different zoom modes. The colors represent from which colored pixel the data comes. Black represents data = 0.

Figure 19: Data from Pixel Array in Normal Mode

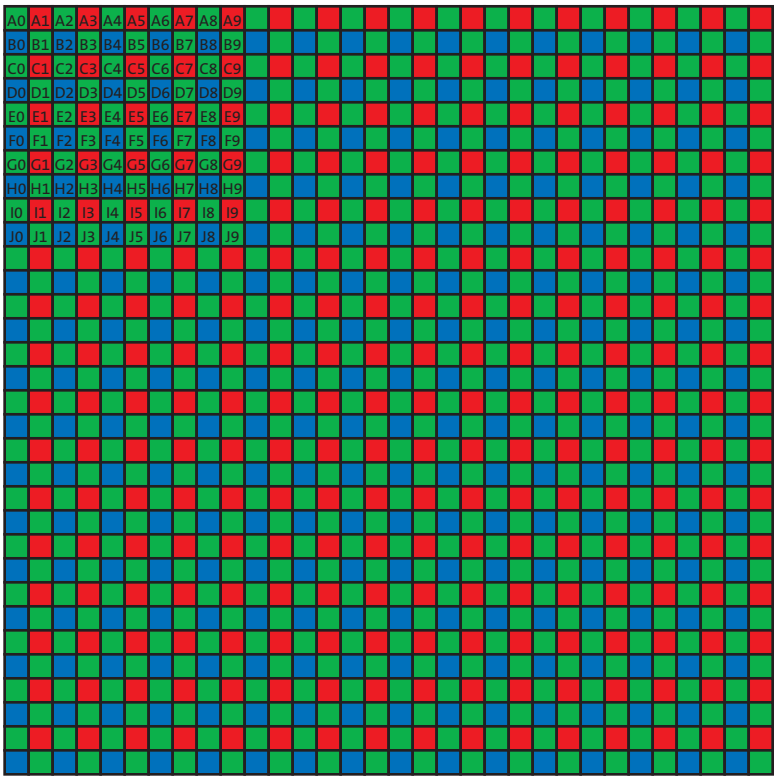


Figure 20: Data from Pixel Array in Zoom 2x Mode

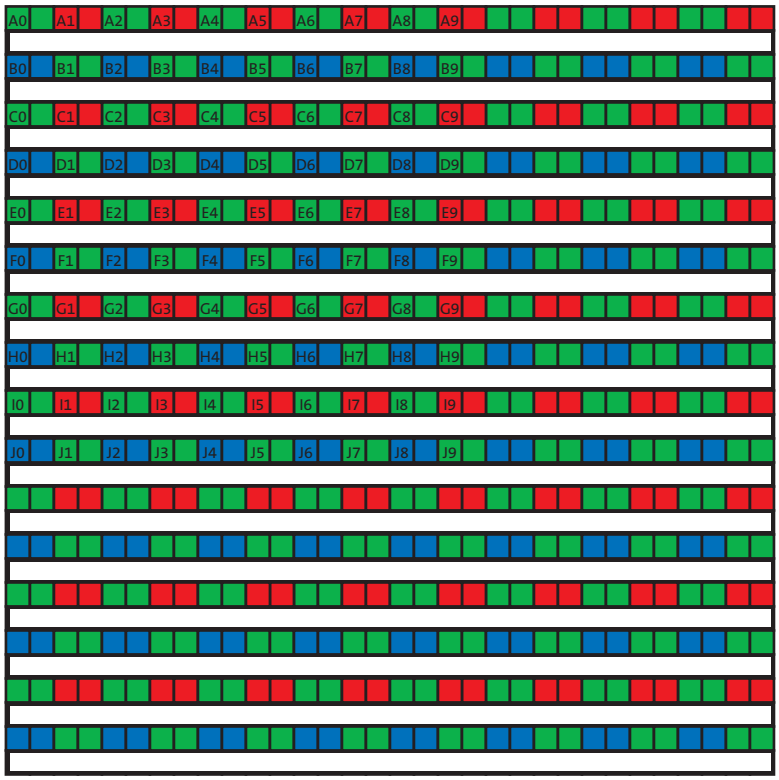


Figure 21: Data from Pixel Array in Zoom 4x Mode

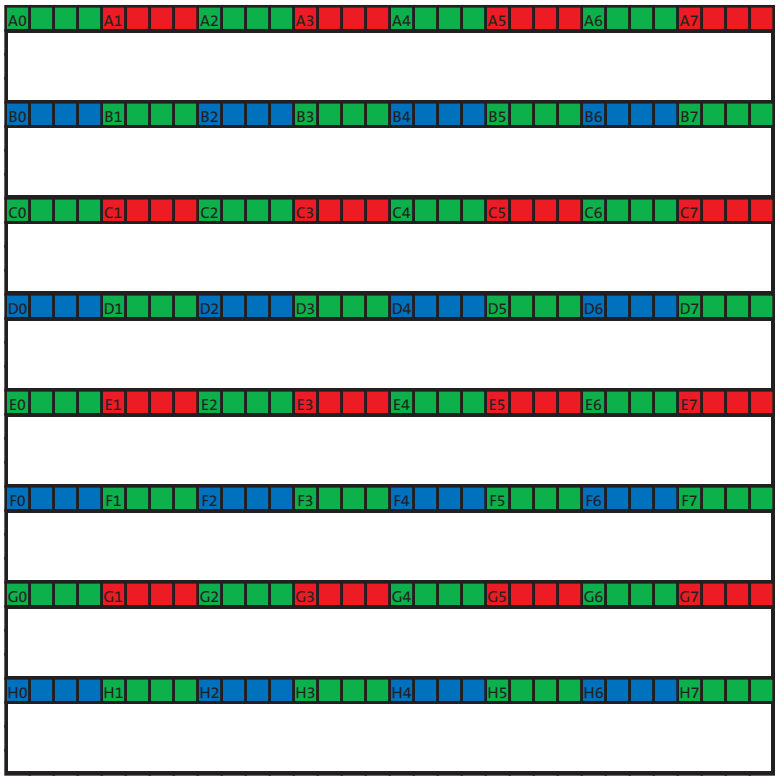


Figure 22: Data from Pixel Array in Zoom 8x Mode

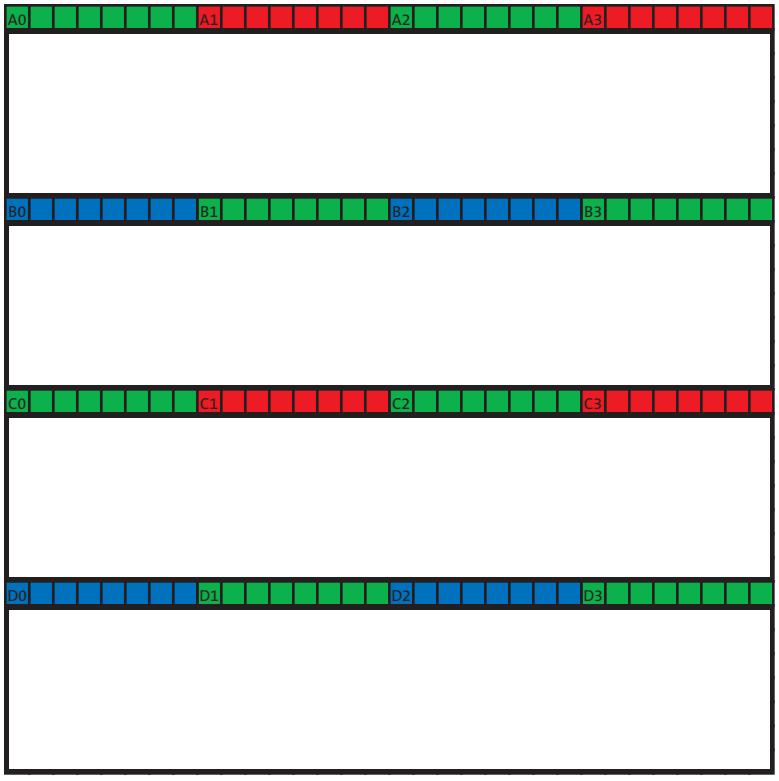
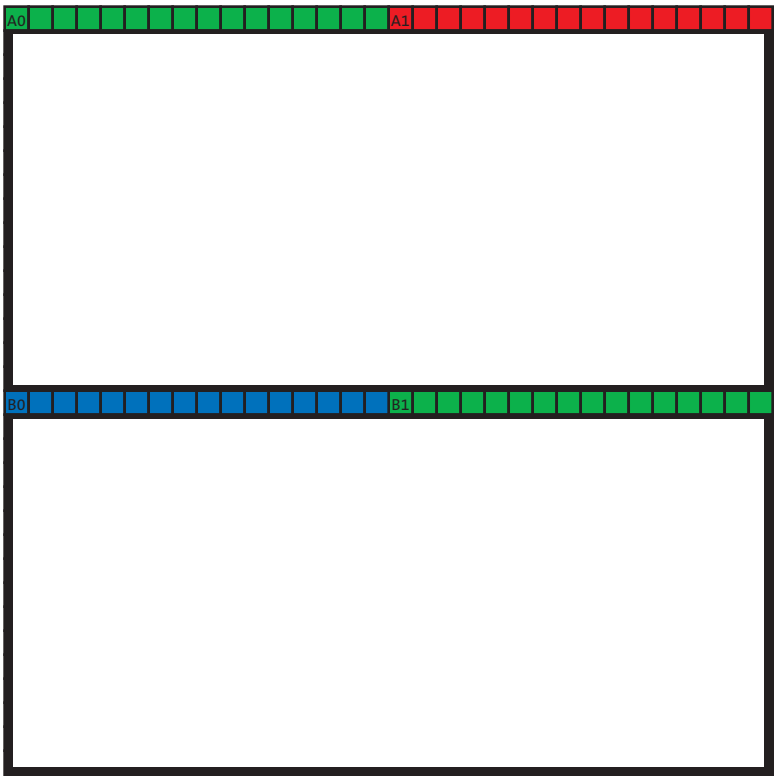


Figure 23: Data from Pixel Array in Zoom 16x Mode



Binning

The MT9D011 supports 2 x 2 binning of four pixels of the same color. This mode can be activated by asserting Reg0x20[15] (Reg0x21 if Context A is used).

Binning is primarily used instead of 2x skip as a way of decimating the picture without losing information. The effect of aliasing in preview mode is eliminated when binning is used instead of just skipping rows and columns.

Activating binning has several implications.

- It adds a level of skip, so the picture that comes out has the same dimensions as a picture read out with the next higher skip setting.
- It increases the minimum hblank and minimum row time requirements (see Table 9 and Table 10).

Binning Limitations

To achieve correct operation, the following conditions must be met:

- Start address must be divisible by four (row and column).
- Window size must be divisible by four in both directions, after dividing by zoom factor and skip factor (because they both reduce the effective window size from the sensor's point of view).

Example: Default row size = 1200. 8x zoom means the actual window on the sensor is divided by 8, so 8x zoom and binning is not allowed with default window size, because 1200 / 8 = 150, which is not divisible by 4.

- Binning can be seen as an extra level of skip. The combination binning/16x skip is therefore not legal.

Frame Rate Control

For a given window size, the blanking registers (Reg0x05-Reg0x08) along with the row speed register (Reg0x0A) can be used to set a particular frame rate.

The frame timing equations (Table 4 and Table 5 on page 13) can be rearranged to express the horizontal blanking or vertical blanking values as a function of the frame rate:

HBLANK_REG = master clock freq / (frame rate*
((Reg0x03/S + BORDER) + VBLANK_REG)*PIXCLK_PERIOD) - (Reg0x04/S + BORDER)

VBLANK_REG = master clock freq / (frame rate*
((Reg0x04/S + BORDER) + HBLANK_REG)*PIXCLK_PERIOD) - (Reg0x03/S + BORDER)

The HBLANK_REG value allows the frame rate to be adjusted with a minimum resolution of one PIXCLK_PERIOD multiplied by the total number of rows (displayed plus blanking). When finer resolution is required, Reg0x0b (Extra Delay) can be used. Reg0x0b allows the frame time to be changed in increments of pixel clocks.

Minimum Horizontal Blanking

The minimum horizontal blanking value is constrained by the time used for sampling a row of pixels and the overhead in the row readout. This is expressed in Table 9.

Table 9: Minimum Horizontal Blanking Parameters

Parameter	Default / 2 ADC Mode, no Binning	1 ADC Mode, no Binning	2 ADC Mode, Binning	1 ADC Mode, Binning
HBLANK(MIN)	286 mclks	324 mclks = 162 pixclks	470 mclks	508 mclks = 254 pixclks

Minimum Row Time Requirement

The total row time must be sufficient to allow all row operations (readout and shutter operations). The row time is the sum of column width (halved during binning divided by column skip factor) and horizontal blanking, and can therefore be adjusted by programming these.

Table 10 shows minimum row time as a function of mode of operation.

Note that this is a particularly strict requirement during binning because twice as many row operations are required per row and the column width is halved.

Table 10: Minimum Row Time Parameters

Parameter	Default / 2 ADC Mode, no Binning	1 ADC Mode, no Binning	2 ADC Mode, Binning	1 ADC Mode, Binning
ROW_TIME(MIN)	473 mclks	488 mclks = 244 pixclks	931 mclks	946 mclks = 473 pixclks
pointer_operations	461 mclks	464 mclks	919 mclks	922 mclks

Context Switching

Reg0xF2 is designed to enable easy switching between sensor modes. Some key registers and bits in the sensor have two physical register locations, called contexts. Bits 0, 1, and 3 of Reg0xF2 control which context register context is currently in use. A "1" in a bit selects Context B, while a "0" selects Context A for this parameter. The select bits can be used in any combination, but by default are setup to allow easy switching between preview mode and full resolution mode:

Context B (Default context)

Reg0xF2	= 0x000B	(Context B)
Reg0x05	= 0x015C	(Horizontal Blanking, Context B)
Reg0x06	= 0x0020	(Vertical Blanking, Context B)
Reg0x20	= 0x0000	(2 ADCs, no column or row skip)

Description: Full-resolution UXGA (1600 x 1200) image at 15 fps

Context A (Alternate context, Preview Mode)

Reg0xF2	= 0x0000	(Context A)
Reg0x07	= 0x00AE	(Horizontal blanking, Context A)
Reg0x08	= 0x0010	(Vertical blanking, Context A)
Reg0x21	= 0x0490	(1 ADC, 2x column and row skip)

Description: Half-resolution SVGA (800 x 600) image at 30 fps

The horizontal blanking and vertical blanking values for the two contexts are chosen so that row time is preserved between contexts. This ensures that changing contexts does not affect integration time. A few more control bits are also available through the context register (Reg0xF2) so that flash and restarting the sensor can be done simultaneously with changing contexts. See Table 2 on page 10 of the MT9D011 register reference for more information.

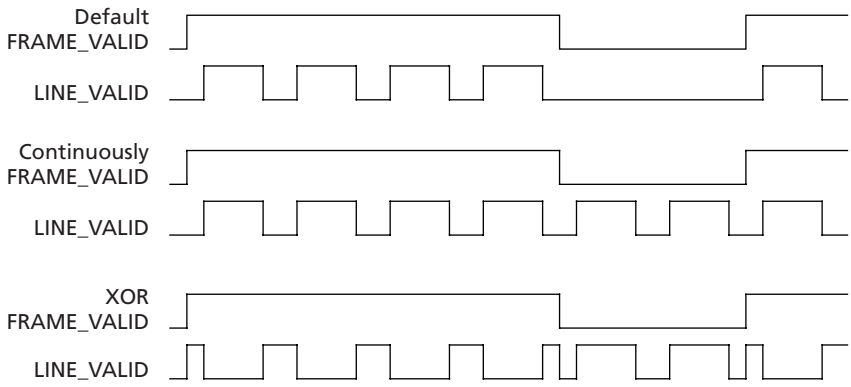
Settings for skip, 1 ADC mode, and binning can be set separately for Context B and Context A using Reg0x20 and Reg0x21, respectively. When these settings are referred to in this document, the register is dependent on what context is set in Reg0xF2.

Valid Data Signals Options

LINE_VALID Signal

By setting bits 14–15 of Reg0x25, the LINE_VALID signal is programmed for three different output formats. The formats shown in Figure 24 illustrate reading out four rows and two vertical blanking rows. In the last format, the LINE_VALID signal is the XOR between the continuous LINE_VALID signal and the FRAME_VALID signal.

Figure 24: LINE_VALID Formats



FRAME_VALID Signal

Reg0x1F allows the user to move FRAME_VALID with respect to data (and LINE_VALID). The rising and falling edges of FRAME_VALID are separately programmable, and can be moved earlier by a number of row_times (plus some overhead).

By programming a value of N in bits [6:0] and enabling it in bit 7, FRAME_VALID will rise before the horizontal blanking N+1 rows earlier. This is shown in Figure 25. N should not be set to higher than 9. Similarly, by programming a value of M in bits [14:8] and enabling it in bit 15, FRAME_VALID will fall M+1 rows earlier. This is shown in Figure 26. M must not be set so FRAME_VALID would fall before LINE_VALID starts toggling. This is avoided by keeping M smaller than Row Width (Reg0x03/S + BORDER).

Figure 25: Early FRAME_VALID Rise

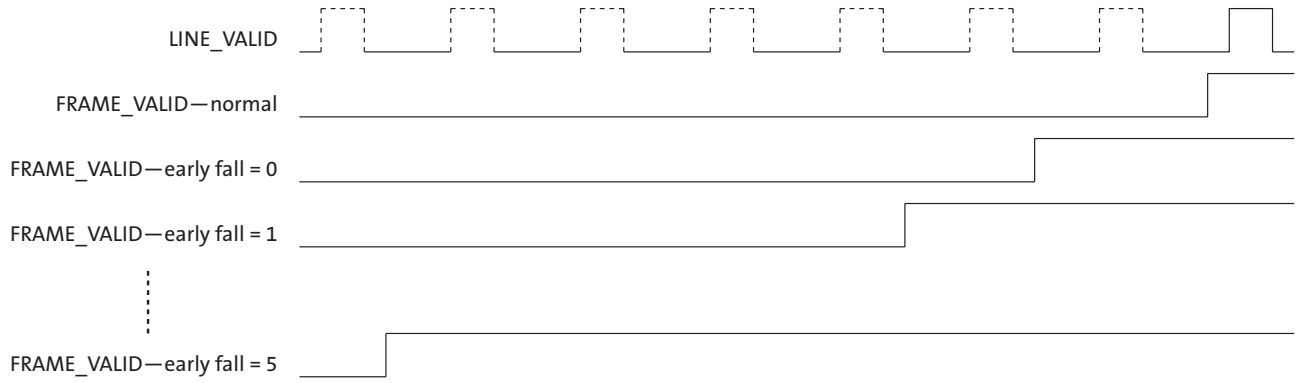
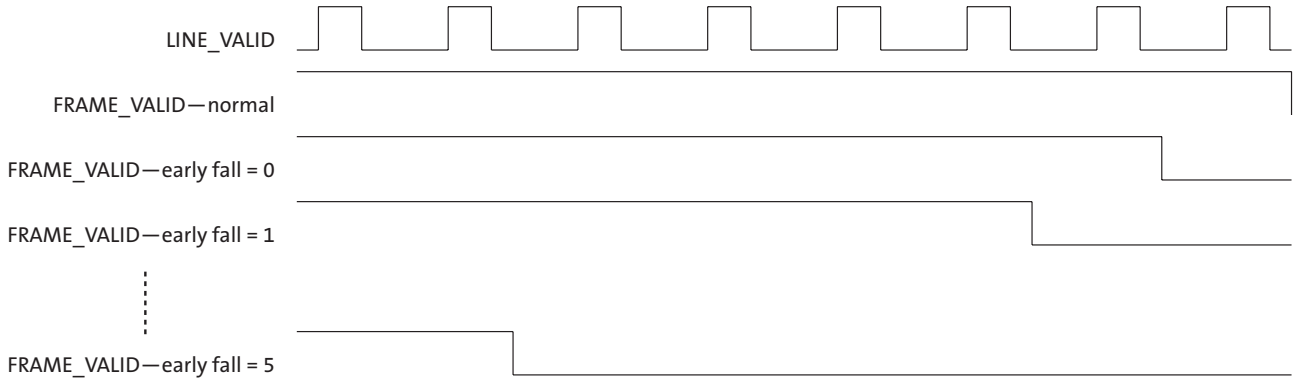


Figure 26: Early FRAME_VALID Fall



Integration Time

Integration time is controlled by Reg0x09 (shutter width in multiples of the row time) and Reg0x0C (shutter delay, in PIXCLK_PERIOD/2). Reg0x0C is used to control sub-row integration times and only has a visible effect for small values of Reg0x09. The total integration time, ^{t}INT, is shown in the equation below:

^{t}INT	=	Reg0x09*Row Time - Integration Overhead - Shutter Delay

where:

Row Time	=	(Reg0x04/S + BORDER + HBLANK_REG)*PIXCLK_PERIOD master clock periods (from Table 4 on page 13)
S	=	Skip Factor, multiplied by 2 if binning is enabled
Overhead Time	=	260 master clock periods (262 in 1 ADC mode)
Shutter Delay	=	Reg0x0C*PIXCLK_PERIOD master clock periods (/2 in 1 ADC mode)

with default settings:

^{t}INT	=	(1232*(1600 + 348)) - 260 - 0
	=	2,399,676 master clock periods = 66.66ms @36 MHz

In the equation, the Integration Overhead corresponds to the delay between the row reset sequence and the row sample (read) sequence.

Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), so that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the sensor adds blanking rows as needed. Additionally, ^{t}INT must be adjusted to avoid banding in the image caused by light flicker. Therefore, ^{t}INT must be a multiple of 1/120 of a second under 60Hz flicker, and a multiple of 1/100 of a second under 50Hz flicker.

Maximum Shutter Delay

The shutter delay can be used to reduce the integration time. A programmed value of *N* reduces the integration time by N master clock periods. The maximum shutter delay is set by the row time and the sample time, as shown in the equation below:

Maximum shutter delay	=	(Row Time - pointer_operations)

where:

Row Time	=	(Reg0x04/S + BORDER + HBLANK_REG)*PIXCLK_PERIOD master clock periods (from Table 4 on page 13)
S	=	Skip Factor, multiplied by 2 if binning is enabled
pointer_operations	=	see Table 10 on page 27.

with default settings:

Maximum shutter delay	=	(1600 + 348) - 461
	=	1487 (master clock periods)

If the value in this register exceeds the maximum value given by this equation, the sensor may not generate an image.

Flash STROBE

The MT9D011 supports both Xenon and LED flash through the FLASH output pin. The timing of the FLASH pin with the default settings is shown in Figure Figure 27, Figure 28, and Figure 29. Reg0x23 allows the timing of the flash to be changed. The flash can be programmed to: fire only once; be delayed by a few frames when asserted; and (for Xenon flash) the flash duration can be programmed.

When Xenon flash is enabled, an integration time significantly smaller than one frame will cause uneven exposure of the image, as will setting a flash pulse width larger than Vertical Blanking.

Enabling the LED flash causes one bad frame in which several rows have the flash on during only part of their integration time. This can be avoided by forcing a restart (write Reg0x0D[1] = 1) immediately after enabling the flash; the first bad frame is then masked out as shown in Figure 29. Read-only bit Reg0x23[14] is set during frames that are correctly integrated; the state of this bit is shown below.

Figure 27: Xenon Flash Enabled

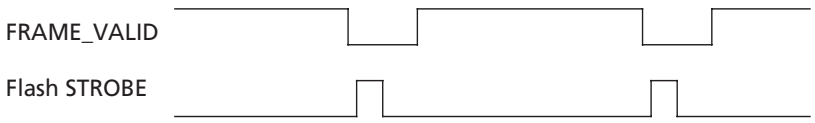
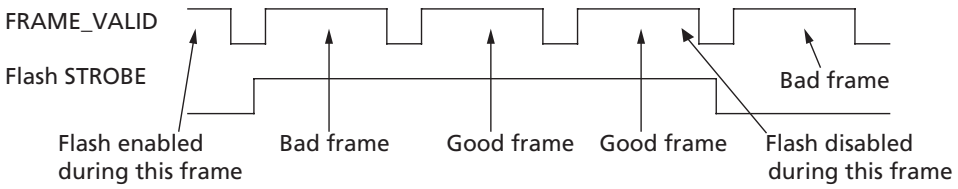
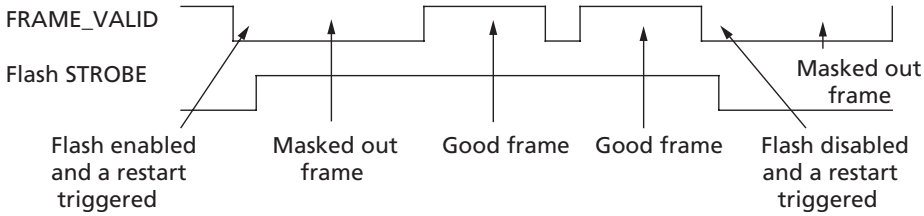


Figure 28: LED Flash Enabled



Note: Integration time = number of rows in a frame.

Figure 29: LED Flash Enabled, Using Restart



Note: Integration time = number of rows in a frame.

Global Reset

The MT9D011 provides a global reset mode in which the pixel integration time is controlled by an external mechanical shutter.

There are two ways of controlling the global reset operation on the MT9D011:

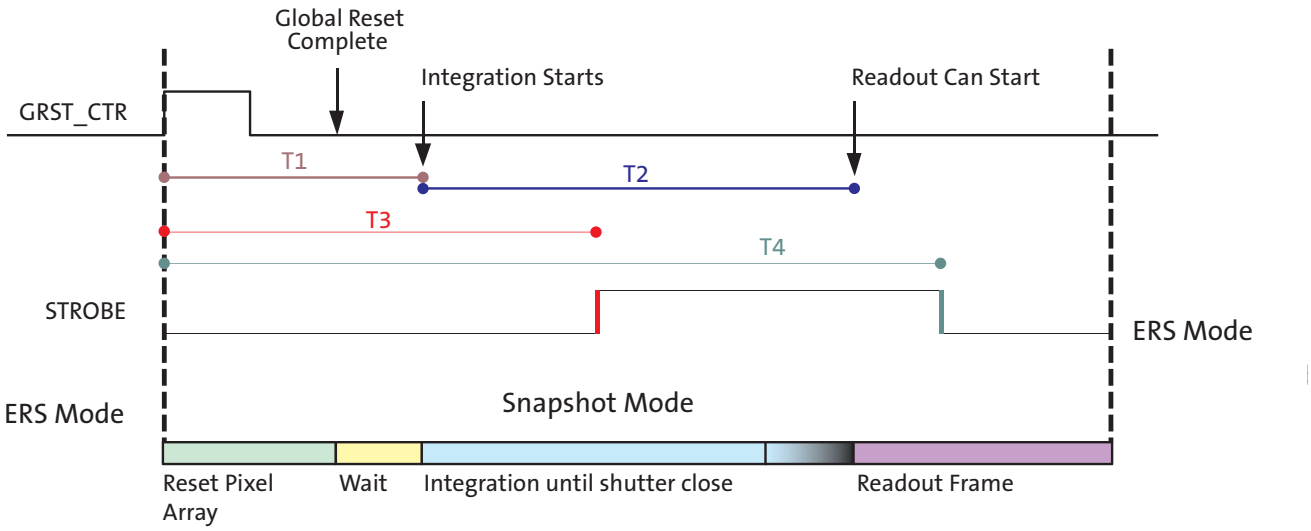
1. By the input pin GRST_CTRL
2. By internal registers

When using method 1, very long integration times can be obtained. When using method 2, the longest integration time that can be programmed is ~400ms when operating at 36 MHz. The exact formula for calculation of the integration time is given later in the document.

The basic operation can be explained using Figure 30. First a short introduction to the registers involved in the control of the global reset sequence:

- Reg0xC0: Global Reset Control
- Reg0xC1: Start Integration Time (T1 on Figure 30)
- Reg0xC2: Start Readout Time (T2 on Figure 30)
- Reg0xC3: Assert Strobe Time (T3 on Figure 30)
- Reg0xC4: De-Assert Strobe Time (T4 on Figure 30)
- Reg0xC5: Assert Flash Time
- Reg0xC6: De-Assert Flash Time

Figure 30: Global Reset Operation



The Reset Phase

A global reset operation is initiated either by a rising edge of the GRST_CTRL pin or writing "1" to Reg0x0C[15]. The following will then happen:

1. The current ERS frame is aborted and Frame Valid will go low.
2. An internal 24-bit counter (CNT24) is reset and starts counting
3. The RST signal will be applied in parallel to all the rows in the pixel array, and the reset phase starts (indicated in green on Figure 30).

The reset phase needs a certain minimum time (20000 master clock cycles) to complete. Integration cannot start before this minimum time has elapsed. This is indicated by the "Global reset complete" arrow on Figure 30.

Depending on the value programmed for T1 in Reg0xC1, two things can now happened:

1. If the 16 Most Significant Bits (MSB) of CNT24 < T1, the pixel array is kept in the reset state (indicated in yellow in Figure 30).
2. If the 16 MSB of CNT24 is >= T1, the reset of the rows is released, and the whole pixel array starts integrating at the same time.

So a programmed value of zero for T1 will force the integration to start at the earliest possible time after initiating the global reset operation. Note that T1 can be used to control the start of the integration even if the global reset operation was initiated by the GRST_CTRL pin.

The Integration Phase

The length of the integration (The blue line on the figure) can be controlled in two ways:

1. Externally by the duration of the GRST_CTRL pulse. This requires that Reg0xC0[0] is set to "1"
2. Internally by T2 (Reg0xC2). Note that the integration time defined by T2 starts from the entry to the integration phase, not the reset phase. The integration time is now defined by the following equation:

T_{int}=(T2*256*master_clock_period)

The maximum allowed value for T2 is 0xDB11 (assuming integration is set to start as early as possible). This gives an integration time of 398.83ms at 36MHz. If T1 is used to delay the start of integration beyond the minimum value (20000*master_clock_period) then maximum allowed value for T2 is reduced accordingly.

The external shutter must be completely closed at the end of the integration period (before readout starts). This is indicated in blue on Figure 30.

The Readout Phase

When integration is complete, Frame Valid goes high and the frame is read out just like in normal ERS mode. The shutter must remain closed during the whole readout. When the last row has been read out, Frame Valid goes low, and the global reset operation is over. The sensor returns to normal ERS operation.

Getting Back to ERS Mode

The first frame after the global reset frame will not have the same integration time for all the rows and should be considered as a bad frame. Depending on how fast the shutter can open again, more bad frames might occur.

When the shutter is guaranteed to be open again after readout of the global reset frame, it is recommended to do a restart by writing to Reg0x0D[1]. The next frame is then guaranteed to have correct exposure.

Synchronization to Mechanical Shutter and Light Source

The MT9D011 provides to programmable output signals (STROBE and FLASH) for the purpose of synchronizing to the mechanical shutter and to an external light source.

They can be seen as two general purpose, fully programmable pins that can generate an arbitrary pulse within the global reset operation, as indicated by the dashed lines on Figure 30.

Programming the STROBE Pin

The rising and falling edge of the STROBE pin is controlled by Reg0xC3 and Reg0xC4. The rising edge will occur when Reg0xC3 = CNT24(23:8). Similar for the falling edge programmed by Reg0xC4. The following applies for the programming of the STROBE pin:

- If Reg0xC0[1] is set to 1, the de-assertion of the STROBE pin is controlled automatically and will occur at the end of the readout independent of the value programmed in Reg0xC4.
- If the rising and the falling edge of STROBE is programmed to occur at the same time, no pulse will be generated.
- The falling edge of STROBE cannot be programmed to occur before the rising edge.

When the integration time (and the start of readout) is controlled externally by the GRST_CTRL pin, the STROBE pin can only be used if it is programmed to be automatically de-asserted after end of readout. If not, the STROBE pin should be disabled by setting and Reg0xC5 - Reg0xC6 to zero.

Programming the FLASH Pin

When entering the global reset operation, the FLASH pin is no longer controlled by the registers that control the FLASH pin during ERS operation (Reg0x23). The rising and falling edge of the FLASH pin is now controlled by Reg0xC5 and Reg0xC6. The rising edge will occur when Reg0xC5 = CNT24(23:8). Similar for the falling edge programmed by Reg0xC6. The following applies for the programming of the FLASH pin:

- If the rising and the falling edge of FLASH is programmed to occur at the same time, no pulse will be generated.
- The falling edge of FLASH cannot be programmed to occur before the rising edge.
- The FLASH pin will always be de-asserted when readout starts (even if the falling edge is programmed to occur after start of readout).

To avoid an extra pulse on the FLASH pin when readout of the global reset frame starts, it is a requirement that if the FLASH pulse in ERS mode is enabled, the programming of it through Reg0x23 should be done such that the "ERS" FLASH pulse is over before the readout of the global frame starts.

When the integration time (and the start of readout) is controlled externally by the GRST_CTRL pin, the FLASH pin should not be used during global reset, and Reg0xC5 - Reg0xC6 should be set to zero.

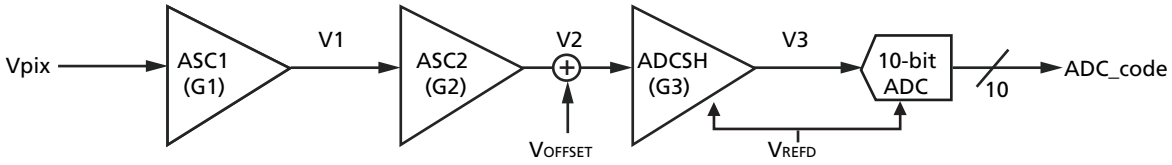
Anti-Eclipse

When a very bright object such as the sun is present in the image, it is possible for a dark spot to appear in the center of the object. This is the so-called “eclipse” effect. The dark spot can be removed by setting Reg0x38 to 0x0826.

Analog Signal Path

The MT9D011 features two identical analog readout channels. A block diagram for one channel is shown in Figure 31. The readout channel consists of two gain stages (ASC1 and ASC2), a sample-and-hold (ADCSH) stage with black level calibration capability (V_{OFFSET}), and a 10-bit ADC.

Figure 31: Analog Readout Channel



Stage-by-Stage Transfer Functions

Transfer functions proceed stage-by-stage, as follows:

Let V_{PIX} be the input of the signal path:	V_{PIX} = pixel output voltage = signal path input voltage,	
The output voltage of ASC 1st stage is:	$V1 = -1*G1*V_{PIX}$	(1)
The output voltage of ASC 2nd stage is:	$V2 = -1*G2*V1$	(2)
The output voltage of ADC Sample-and-Hold stage is:	$V3 = 2*G3*V2 - V_{REFD} + V_{OFFSET}$	(3)
and the ADC output code is:	$ADC\ output\ code = 511*(1 + (V3 / V_{REFD}))$	(4)

From (1) to (4), the ADC output code can also be written as: $ADC\ code = (1022/V_{REFD})*[G1*G2*G3*V_{PIX} + (Voffset/(2*G3))]$ (5)

Where G1, G2, and G3 are the gain settings, V_{OFFSET} is the offset (calibration) voltage, and V_{REFD} is the reference voltage of the ADC. The gain setting G3 is applied to the signal but is not applied to V_{OFFSET}. The parameters V_{REFD}, G1, G2, G3, and V_{OFFSET} are described next.

VREFD

The V_{REFD} parameters are as follows:

The ADC reference voltage V_{REFD} is: $V_{REFD} = V_{REF\_HI} - V_{REF\_LO}$ (6)

where $V_{REF\_HI} = 55.5mV*(Reg0x41[7:4] + 23)$ (7)

using default register values: $V_{REF\_HI} = 55.5mV*(13 + 23) = 1.998V$

and $V_{REF\_LO} = 55.5mV*(Reg0x41[3:0] +11)$ (8)

using default register values: $V_{REF\_LO} = 55.5mV*(7 +11) = 0.999V$

so $V_{REFD} = 55.5mV*(Reg0x41[7:4] - Reg0x41[3:0] + 12)$ (9)

using default register values $V_{REFD} = 1.998 - 0.999 = 0.999V$

Gain Settings: G1, G2, G3

The gains for green1, blue, red, and green2 pixels are set by registers Reg0x2B, Reg0x2C, Reg0x2D, and Reg0x2D, respectively. Gain can also be globally set by Reg0x2F. The analog gain is set by bits 8:0 of the corresponding register as follows:

G1 = bit 7 + 1 (10)

G2 = bit 6:0 / 32 (11)

G3 = bit 8 + 1 (12)

Digital gain is set by bits 11:9 of the same registers.

Offset Voltage: VOFFSET

The offset voltage provides a constant offset to the ADC to fully utilize the ADC input dynamic range. The offset voltages for green1, blue, red, and green2 pixels are manually set by registers Reg0x61, Reg0x62, Reg0x63, and Reg0x64, respectively. Note that the offset voltages also can be automatically set by the black- level calibration loop.

For a given color, the offset voltage, V_{OFFSET}, is determined by:

$V_{OFFSET} = 0.50V*offset\_gain*offset\_sign*offset\_code[7:0]/255$ (13)

where: "offset_sign" is determined by bit 8 as:

if bit 8 = 0, offset_sign = +1 (14)

if bit 8 = 1, offset_sign = -1 (15)

"offset_code" is the decimal value of bit<7:0>

"Offset_gain" is determined by the 2-bit code from Reg0x5A[1:0], as shown in Table 11. These step sizes are not exact; increasing the stage0 ADC gain from 2 to 4 decreases the step size significance; decreasing the ADC VREFD increases the step size significance.

Table 11: Offset Gain

Reg0x5A[1:0]	Offset_Gain
00	OFFSET_GAIN = 0 (no calibration voltage is applied)
01	OFFSET_GAIN = 0.25 (1 calibration LSB is equal to 0.5 ADC LSB when VREFD = 1V)
10	OFFSET_GAIN = 0.50 (1 calibration LSB is equal to 1 ADC LSB when VREFD = 1V)
11	OFFSET_GAIN = 1 (1 calibration LSB is equal to 2 ADC LSB when VREFD = 1V)

Recommended Gain Settings

The analog gain circuitry in the MT9D011 provides signal gains from 1 to 15.875.

Table 12: Recommended Gain Settings

Desired Gain	Recommended Gain Register Setting
1–1.969	0x020–0x03F
2–7.938	0x0A0–0x0FF
8–15.875	0x1C0–0x1FF

By applying maximum analog and digital gain, it is possible to achieve a total gain of 128. It is not recommended to operate the sensor with such high gain since this may introduce visible noise in the image. Digital gain should therefore be limited to a factor of 2 in order to keep the total gain below 32x.

Output Enable Control

When the sensor is configured to operate in Default mode, the DOUT, FRAME_VALID, LINE_VALID, PIXCLK, and flash outputs can be placed in a high-impedance state under hardware or software control, as shown in Table 13.

Table 13: Output Enable Control

Standby	Reg0x0D[4] (output_dis)	Reg0x0D[6] (drive_pins)	Pin State
0	0 (default)	0 (default)	Driven
1	0 (default)	0 (default)	High-Z
don't care	0 (default)	1	Driven
don't care	1	don't care	High-Z

The pin transition between driven and High-Z always occurs asynchronously. Output-enable control is provided as a mechanism to allow multiple sensors to share a single set of interface pins with a host controller.

Note: There is no benefit in placing the pins in a High-Z while the sensor is in its low power standby state. Therefore, in single-sensor applications that use the STANDBY pin to enter and leave the standby state, programming Reg0x0D[6] = 1 is recommended.

Power-Saving Modes

The sensor can be placed in a low power standby state by either of these mechanisms:

- Asserting STANDBY input pin (provided that Reg0x0D[7] = 0)
- Setting Reg0x0D[2] = 1 by performing a register write through the serial register interface.

These two methods are equivalent and have the same effect:

- The source of standby is synchronized and latched. Once latched, the full standby sequence is completed even if the source of standby is removed.
- The readout of the current row is completed.
- Internal clocks are gated off.
- The analog signal chain and associated current and voltage sources are placed in a low power state.

The standby state is maintained for as long as the standby source remains asserted. Table 14 shows the state of the pin interface while in standby state.

Table 14: Signal State During Standby

Signal	State
LINE_VALID	0
FRAME_VALID	0
STROBE	0
PIXCLK[1]	0
FLASH	0
DOUT9–DOUT0	0

[1]The state of the PIXCLK output during standby is dependent on the setting of bit 10 in the Read Mode register for the current context (Reg0x020 or Reg0x21) when entering standby. In 1 ADC mode (power mode) the logic state of PIXCLK is "1" during standby while in 2 ADC mode (default) the logic state is "0."

Output-enable control can be used to place the pin interface in a high-impedance state (see "By applying maximum analog and digital gain, it is possible to achieve a total gain of 128. It is not recommended to operate the sensor with such high gain since this may introduce visible noise in the image. Digital gain should therefore be limited to a factor of 2 in order to keep the total gain below 32x." on page 37).

While in standby, the state of the internal registers is maintained and the sensor continues responding to accesses through its serial register interface. An even lower power standby state can be achieved by stopping the input clock (CLKIN) while in standby. If the input clock is stopped, the sensor does not respond to accesses through its serial register interface.

Exit from standby must be through the same mechanism as entry to standby. When the standby source is negated, this sequence occurs:

1. The internal clocks are restarted.
2. The analog circuitry is restored to its normal operating state.
3. The timing and control circuitry performs a restart equivalent to writing Reg0x0D[1] = 1.

After this sequence is complete, normal operation resumes. If the input clock is stopped during standby, it must be restarted before leaving standby.

PLL and Standby

If the PLL is used to generate master clock, special care must be taken when entering standby mode. The PLL uses relatively high power, so allowing the PLL to power down during standby is recommended. This can be controlled in Reg0x65[13]. By default the PLL powers down whenever MT9D011 enters standby. The operation of the circuit cannot be guaranteed if the PLL is driving the master clock when it powers down.

To safely allow the PLL to power down when entering standby, turn on PLL bypass before triggering standby (controlled by Reg0x65[15]). When coming out of standby mode, the normal PLL power-up sequence must be followed as specified in "PLL Power-up" on page 19.

Floating Inputs

Many MT9D011 signals use bi-directional pins (shown in Table 5 on page 13) for the following three reasons:

- The signal associated with the pin is bi-directional in normal use (the only signal in this category is SDATA).
- The pin is normally used as an output, but is used as an input during manufacturing test modes (e.g., DOUT[9:0]).
- Standard design practice dictates that signal inputs should not be allowed to float for long periods of time.

This leads to two areas where the design application should be reviewed:

- When using the output-enable control. All MT9D011 bi-directional pins that enter a high-impedance state must be driven to a valid logic level. (See "By applying maximum analog and digital gain, it is possible to achieve a total gain of 128. It is not recommended to operate the sensor with such high gain since this may introduce visible noise in the image. Digital gain should therefore be limited to a factor of 2 in order to keep the total gain below 32x." on page 37.)
- When input pins are allowed to float. The MT9D011 does not include on-chip pull-down resistors, therefore, no input pins should be allowed to float.

Dark Row/Column Display

Optically black rows 4 through 11are used to provide data for black level calibration and are not normally visible in the displayed image. Setting Reg0x22[7] = 1 makes these rows visible in the displayed image. This is achieved by asserting FRAME_VALID earlier than normal, and keeping it asserted longer, so that the following rows are displayed:

- The optically black rows at the start of the pixel array (controlled by Reg0x22[2:0]).
- Two rows before the visible rows.
- The visible rows (controlled by Reg0x01, Reg0x03 and Reg0x20).

The result of setting Reg0x22[7] = 1 is a larger image (more rows) than is programmed by Reg0x03.

Optically black columns 4 through 43 are used to provide data for row-wise noise cancellations, depending on certain settings. These pixels are not normally visible in the displayed image.

- Set Reg0x22[8] = 0 (to disable readout of the dark columns); set Reg0x30[10] = 0 (to disable row-wise correction); then adjust Reg0x02.
- Set Reg0x22[9] = 1. When Reg0x22[9] = 1, LINE_VALID is asserted a number of pixel clocks earlier than normal. Data from the dark columns (20 or 36 columns), depending on Reg0x22[10] is followed by two pixel clocks of undefined data, then by data from the visible columns (controlled by Reg0x02, Reg0x04, and Reg0x20).

Clock Control

The MT9D011 uses an aggressive clock-gating methodology to reduce power consumption: the clocked logic is divided into a number of separate domains, each of which is only clocked as required. Reg0x65 can be used to bypass the clock gating, so that clocks to individual domains run continuously.

When the MT9D011 enters a low power state, almost all of the internal clocks are "gated off." The only exception is that a small amount of logic (approximately 10 flip-flops) is clocked so that access to the two-wire serial interface continues to function correctly. See "Power-Saving Modes" on page 37 for more information.

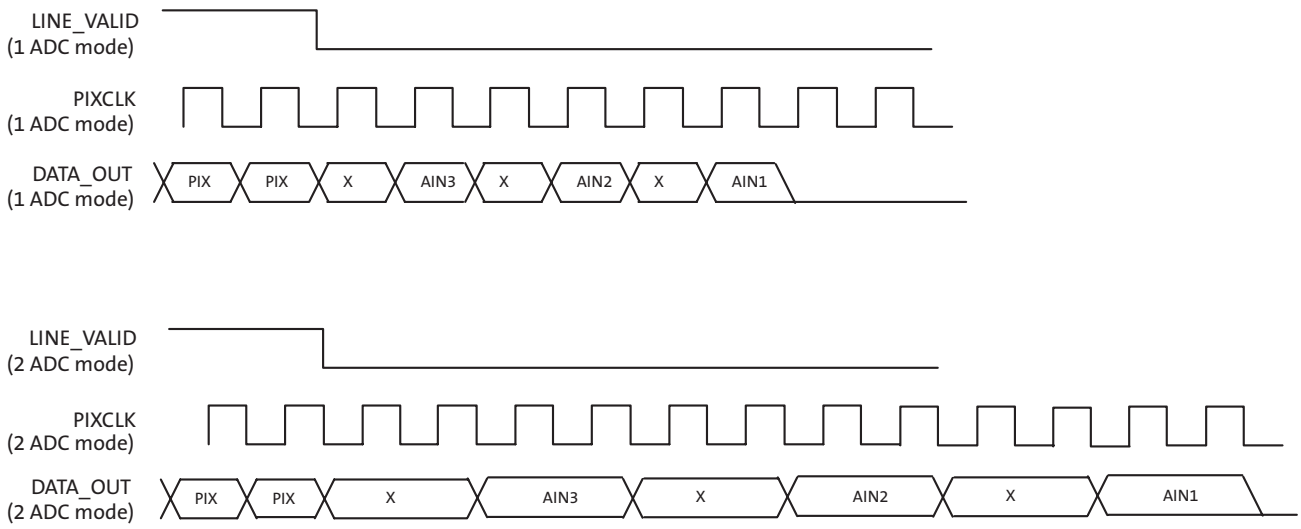
Analog Inputs AIN1–AIN3

MT9D011 can share its on-chip ADC resources, such as for use in auto focus applications. If Reg0xE3[15] is set, the chip samples AIN1–AIN3 once per row (after reading out the data from the row). The digital data from this sampling is available to the user in two ways:

- Data can be read in registers Reg0xE0 to Reg0xE2
- Data is present in the data stream after LINE_VALID goes low if Reg0xE3[14] is set

The nominal range of the AIN pins are 0V + VOFFSET to VREFD + VOFFSET. VREFD is the ADC reference voltage (nominally 1V), but can be programmed. (See "Analog Signal Path" on page 35.) VOFFSET is the offset in the ADC and is typically ±10mV to 20mV. If required, the offset can be measured by converting a calibrated reference voltage, which can be used to compensate at the input. The ADC is designed to operate with differential inputs. Since AIN1-AIN3 are used as single-ended inputs to the ADC, it is recommended to average values from several samples (if possible, a whole frame) to cancel out noise.

Figure 32: Timing Diagram AIN1–AIN3 Sample



Power-up Sequence

There are no specific requirements to the order in which different supplies are turned on. The reset sequence cannot start before the last supply is stable within the valid ranges as defined in Table 17: DC Electrical Characteristics on page 43.

Hard Reset Sequence

After power-up, a hard reset is required. Assuming all supplies are stable, the assertion of the RESET# pin to logic “0” will set device in reset mode ~30ns after assertion. The input clock does not have to run while RESET# is active. Release of RESET# will require that the clock is running and after 3 clock cycles (CLKIN), the serial interface is ready to accept commands on the two-wire serial interface.

Soft Reset Sequence

At any time during normal operation or standby, the user can do a soft reset by writing a logic "1" to Reg0x0D[0] using the two-wire serial interface. This will also put the device in reset mode and all registers (including PLL state and settings) will get their default values. Writing a logic "0" to the same register will release the soft reset, and normal operation can be resumed once the write operation on the serial interface is completed.

Electrical Specifications

Recommended operating temperature range is from –20°C to +55°C. The sensor image quality may degrade avove +55C.

Table 15: AC Electrical Characteristics

Symbol	Definition	Condition	MIN	TYP	MAX	Units
f_{CLKIN1}	Input Clock Frequency	PLL enabled	4	36	40	MHz
t_{CLKIN1}	Input clock period	PLL enabled	250	27.8	25	ns
f_{CLKIN2}	Input clock frequency	PLL enabled	4	36	40	MHz
t_{CLKIN2}	Input clock period	PLL enabled	250	27.8	25	ns
t_R	Input clock rise time		0.5		1	V/ns
t_F	Input clock fall time		0.5		1	V/ns
	Clock Duty Cycle		40	50	60	%
t_{CP}	CLKIN to PIXCLK propagation delay				40	MHz
f_{PIXCLK}	PIXCLK frequency	Default				ns
t_{PD}	PIXCLK to data valid	Default	–3		3	ns
t_{PFH}	PIXCLK to Frame_Valid HIGH	Default	–3		3	ns
t_{PLH}	PIXCLK to Line_Valid HIGH	Default	–3		3	ns
t_{PFL}	PIXCLK to Frame_Valid LOW	Default	–3		3	ns
t_{PLL}	PIXCLK to Frame_Valid LOW	Default	–3		3	ns
C_{IN}	Input Pin Capacitance			3.5		pF
C_{LOAD}	Load Capacitance			15	20	pF
AC Setup Conditions						
	f_{CLKIN1}		4	36	40	MHz
	V_{DD}		1.7	1.8	1.9	V
	V_{DDQ}		1.7	2.8	3.1	V
	V_{AA}		2.5	2.8	3.1	V
	VAAPIX		2.5	2.8	3.1	V
	VDDPLL		2.5	2.8	3.1	V
	Output load			15		pF

Table 16: Absolute Maximum Ratings

Symbol	Parameter	Rating			Unit
		MIN	TYP	MAX	
V_{DD}	Core Digital Voltage	1.7	1.8	1.9	V
V_{DDQ}	I/O Digital Voltage	1.7	2.8	3.1	V
V_{AA}	Analog Voltage	2.5	2.8	3.1	V
VAAPIX	Pixel Supply Voltage	2.5	2.8	3.1	V
VDDPLL	PLL Supply Voltage	2.5	2.8	3.1	V
T_{OP}	Operating Temperature	–30	55	70	°C
T_{STG}[1]	Storage Temperature	–40		125	°C

Note: 1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 17: DC Electrical Characteristics

Symbol	Definition	Conditions	MIIN	TYP	MAX	Units
V_{IH}	Input High Voltage	V_{DDQ} = 2.8	2.4		V_{DDQ}+0.3	V
		V_{DDQ} = 1.8	1.4		V_{DDQ}+0.3	
V_{IL}	Input Low Voltage	V_{DDQ} = 2.8	GND-0.3		0.8	V
		V_{DDQ} = 1.8	GND-0.3		0.5	
I_{IN}	Input Leakage Current	No pull-up resistor; V_{IN} = V_{DDQ}or D_{GND}	-2		2	µA
V_{OH}	Output High Voltage	At specified for I_{OH}	V_{DDQ}-0.4			V
V_{OL}	Output Low Voltage	At specified for I_{OL}			0.4	V
I_{OH}	Output high current	At specified V_{OH} = V_{DD}-400mV	-7			mA
I_{OL}	Output low current	At specified V_{OL} = 400mV	-7			mA
I_{OZ}	Tri-state Output Leakage Current	V_{IN} = V_{DDQ} or GND	-2		2	µA
IDD1	Digital Operating Current	PIXCLK=f_{CLKIN}1Context B		4.7		mA
IDDQ1	I/O Digital Operating Current	PIXCLK=f_{CLKIN}1Context B, CLOAD = 15pF		5.2		mA
IAA1	Analog Operating Current	PIXCLK=f_{CLKIN}1Context B		41.5		mA
IAAPIX1	Pixel Supply Current	PIXCLK=f_{CLKIN}1Context B		2.0		mA
IDDPLL1	PLL Supply Current	PIXCLK=f_{CLKIN}1Context B, CLKIN=48 MHz, M=28, N=0, P-1		1.65	7	mA
IDD2	Digital Operating Current	PIXCLK=f_{CLKIN}1/2 Context A		3.0		mA
IDDQ2	I/O Digital Operating Current	PIXCLK=f_{CLKIN}1/2 Context A, CLOAD=15pF		3.6		mA
IAA2	Analog Operating Current	PIXCLK=f_{CLKIN}1/2 Context A		23		mA
IAAPIX2	Pixel Supply Current	PIXCLK=f_{CLKIN}1/2 Context A		2.0		mA
IDDPLL2	PLL Supply Current	PIXCLK=f_{CLKIN}1/2 Context A, CLKIN=48 MHz, M=28, N=0, P=1		1.65		mA
ISTDBY1	Standby Current PLL enabled	PLL enabled at 25C			10	µA
ISTDBY2	Standby Current PLL disabled	PLL disabled at 25C			10	µA

Two-wire Serial Bus Timing Parameters

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 33: Two-wire Serial Bus Timing Parameters

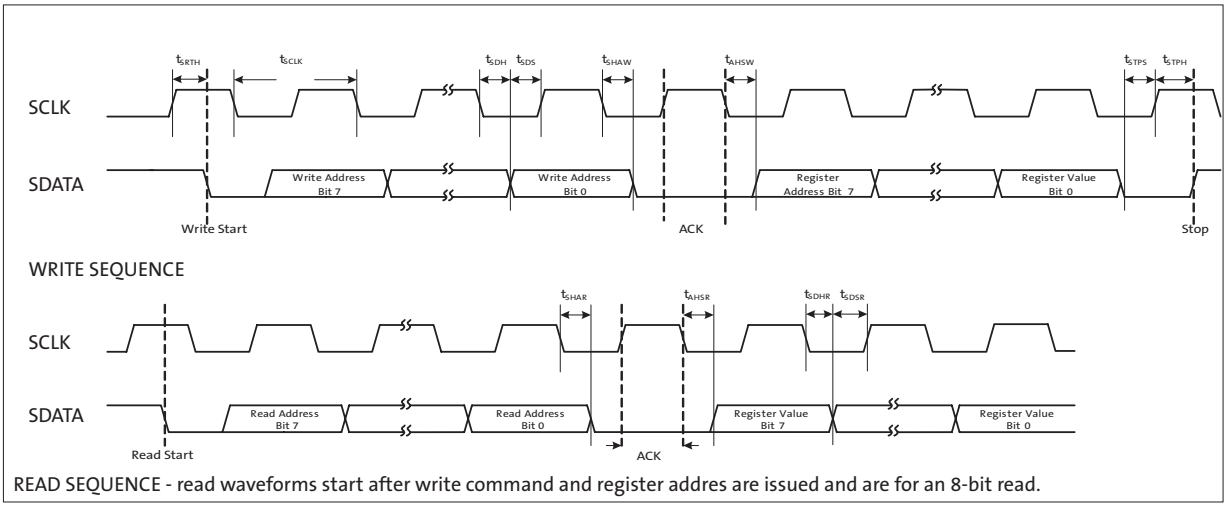


Table 18: Two-Wire Serial Bus Characteristics

Symbol	Definition	Condition	MIN	TYP	MAX	Units
f_{SCLK}	Serial interface input clock frequency				$f_{CLK}/16$	kHz
t_{SCLK}	Serial interface input clock period					
	SCLK Duty Cycle		40	50	60	%
t_{SRTH}	Start Hold Time	WRITE/READ				t_{CLKIN}
t_{SDH}	SDATA Hold	WRITE				t_{CLKIN}
t_{SDS}	SDATA Setup	WRITE				t_{CLKIN}
t_{SHAW}	SDATA HOld to ACK	WRITE				t_{CLKIN}
t_{AHSW}	ACK Hold to SDATA	WRITE				t_{CLKIN}
t_{STPS}	Stop Setup Time	WRITE/READ				t_{CLKIN}
t_{STPH}	Stop Hold Time	WRITE/READ				t_{CLKIN}
t_{SHAR}	SDATA Hold to ACK	READ				t_{CLKIN}
t_{AHSR}	ACK Hold to SDATA	READ				t_{CLKIN}
t_{SDHR}	SDATA Hold	READ				t_{CLKIN}
t_{SDSR}	SDATA Setup	READ				t_{CLKIN}
C_{IN_SI}	Serial interface input pin capacitance			3.5		pF
C_{LOAD_SD}	SDATA Max Load Capacitance			15		pF
R_{SD}	SDATA pull-up resistor			1.5		KΩ

Figure 34: Default Data Output Timing Diagram

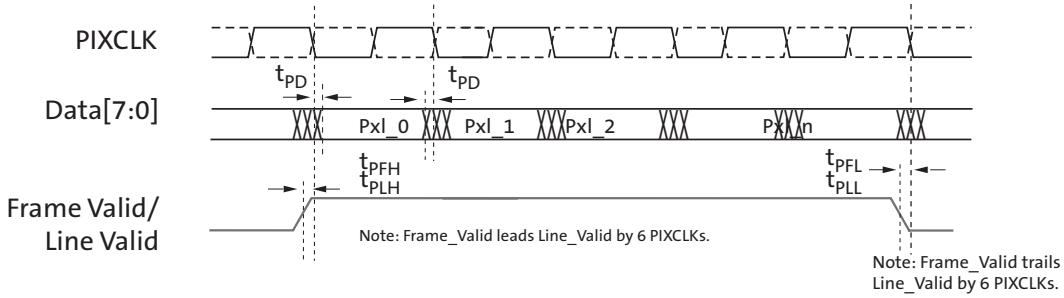
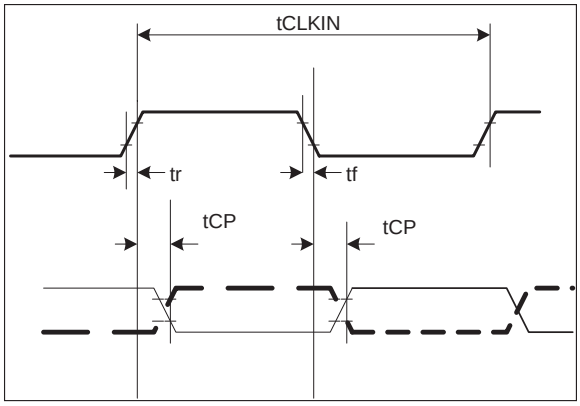


Figure 35: Propagation Delay



Revision History

Rev. E 2/10

Updated to Aptina template

Rev. D, Preliminary 2/06

- Update Table 15, “AC Electrical Characteristics,” on page 42

Rev. C, Preliminary 1/06

- Add Table 2, “Available Part Numbers,” on page 1
- Update Table 15, “AC Electrical Characteristics,” on page 42

Rev. B, Preliminary 5/05

- Update Table 1 on page 1
- Update Figure 2 on page 7
- Update Table 7 on page 14
- Updated Table 8 on page 20
- Update Table 14 on page 38
- Replace “Global Reset” on page 32
- Added “Anti-Eclipse” on page 35
- Update Table 17 on page 43
- Update Table 18 on page 44
- Add Figure 34 on page 45
- Update Figure 35 on page 45

Rev. A, Preliminary 11/04

- Initial release of document

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Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.