SONY

ICX429ALL

Diagonal 8mm (Type 1/2) CCD Image Sensor for CCIR B/W Video Cameras

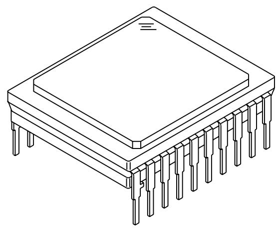
Description

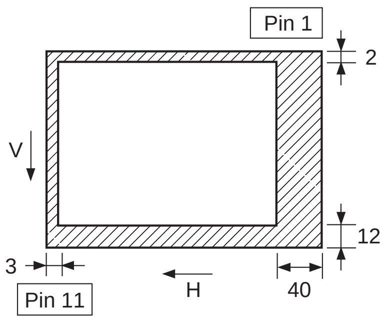
The ICX429ALL is an interline CCD solid-state image sensor suitable for CCIR B/W video cameras with a diagonal 8mm (Type 1/2) system. Basic characteristics such as sensitivity, smear, dynamic range and S/N are improved drastically through the adoption of EXview HAD CCD™ technology.

This chip features a field period readout system and an electronic shutter with variable charge-storage time. This chip is compatible with the pins of the ICX249AL and has the same drive conditions.

EXview HAD CCD™ has differrent spectral characteristics from the curreent CCD.

20 pin DIP (Cer-DIP)





Optical black position
(Top View)

Features

- High sensitivity
- Low smear
- High D range (+1dB compared with the ICX249AL)
- High S/N
- High resolution and low dark current
- Excellent antiblooming characteristics
- Continuous variable-speed shutter
- Substrate bias: Adjustment free (external adjustment also possible with 6 to 14V)
- Reset gate pulse: 5Vp-p adjustment free (drive also possible with 0 to 9V)
- Horizontal register: 5V drive

Device Structure

- Interline CCD image sensor
- Optical size: Diagonal 8mm (Type 1/2)
- Number of effective pixels: 752 (H) × 582 (V) approx. 440K pixels
- Total number of pixels: 795 (H) × 596 (V) approx. 470K pixels
- Chip size: 7.40mm (H) × 5.95mm (V)
- Unit cell size: 8.6µm (H) × 8.3µm (V)
- Optical black: Horizontal (H) direction: Front 3 pixels, rear 40 pixels
  Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 22
  Vertical 1 (even fields only)
- Substrate material: Silicon

***EXview* HAD CCD**™

* EXview HAD CCD is a trademark of Sony Corporation.
EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation-Diode) sensor.

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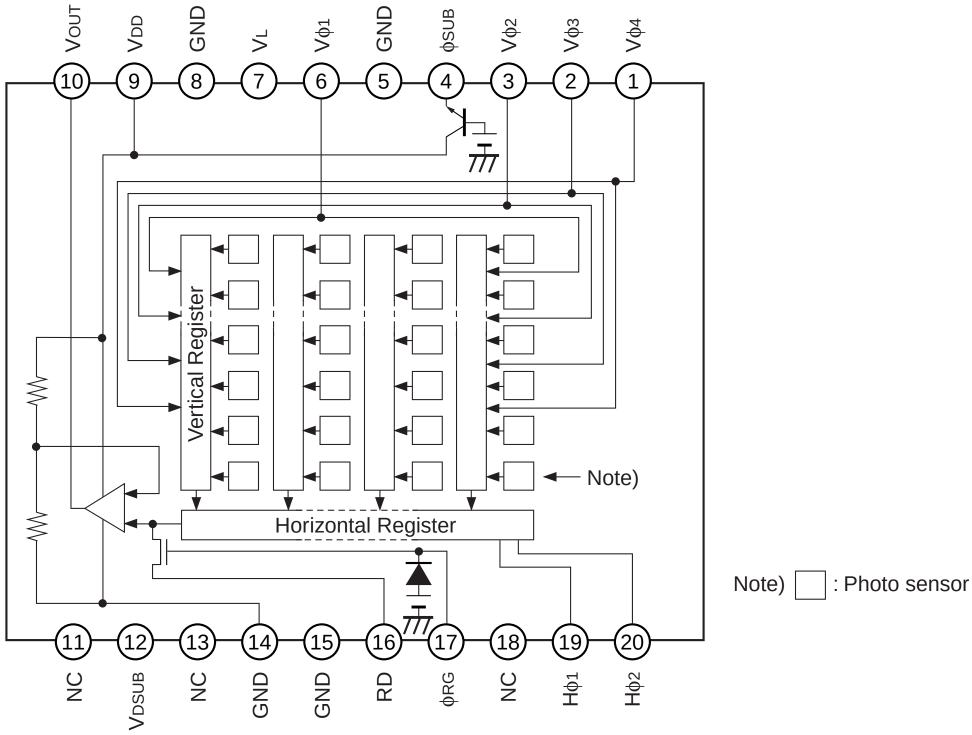
Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	11	NC	
2	$V\phi_3$	Vertical register transfer clock	12	V_{DSUB}	Substrate bias circuit supply voltage
3	$V\phi_2$	Vertical register transfer clock	13	NC	
4	ϕ_{SUB}	Substrate clock	14	GND	GND
5	GND	GND	15	GND	GND
6	$V\phi_1$	Vertical register transfer clock	16	RD	Reset drain bias
7	V_L	Protective transistor bias	17	ϕ_{RG}	Reset gate clock
8	GND	GND	18	NC	
9	V_{DD}	Output circuit supply voltage	19	$H\phi_1$	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	$H\phi_2$	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate clock ϕ_{SUB} – GND		–0.3 to +50	V	
Supply voltage	V_{DD}, V_{RD}, V_{DSUB}, V_{OUT} – GND	–0.3 to +18	V	
	V_{DD}, V_{RD}, V_{DSUB}, V_{OUT} – ϕ_{SUB}	–55 to +10	V	
Clock input voltage	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – GND	–15 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – ϕ_{SUB}	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizontal clock input pins		to +17	V	
$H\phi_1$, $H\phi_2$ – $V\phi_4$		–17 to +17	V	
ϕ_{RG} – GND		–10 to +15	V	
ϕ_{RG} – ϕ_{SUB}		–55 to +10	V	
V_L – ϕ_{SUB}		–65 to +0.3	V	
Pins other than GND and ϕ_{SUB} – V_L		–0.3 to +30	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*1 +27V (Max.) when clock width < 10μs, clock duty factor < 0.1%.

Bias Conditions 1 [when used in substrate bias internal generation mode]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit supply voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Protective transistor bias	V_L		*1			
Substrate bias circuit supply voltage	V_{DSUB}	14.55	15.0	15.45	V	
Substrate clock	ϕSUB		*2			

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same supply voltage as the V_L power supply for the V driver should be used. (When CXD1267AN is used.)

*2 Do not apply a DC bias to the substrate clock pin, because a DC bias is generated within the CCD.

Bias Conditions 2 [when used in substrate bias external adjustment mode]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit supply voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Protective transistor bias	V_L		*3			
Substrate bias circuit supply voltage	V_{DSUB}		*4			
Substrate voltage adjustment range	V_{SUB}	6.0		14.0	V	*5
Substrate voltage adjustment precision	ΔV_{SUB}	–3		+3	%	*5

*3 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same supply voltage as the V_L power supply for the V driver should be used. (When CXD1267AN is used.)

*4 Connect to GND or leave open.

*5 The setting value of the substrate voltage (V_{SUB}) is indicated on the back of the image sensor by a special code. When adjusting the substrate voltage externally, adjust the substrate voltage to the indicated voltage. The adjustment precision is ±3%. However, this setting value has not significance when used in substrate bias internal generation mode.

V_{SUB} code — one character indication

Code and optimal setting correspond to each other as follows.

V_{SUB} code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W
Optimal setting	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0

<Example> "L" → V_{SUB} = 9.0V

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit supply current	I_{DD}		5.0	10.0	mA	

Clock Voltage Conditions

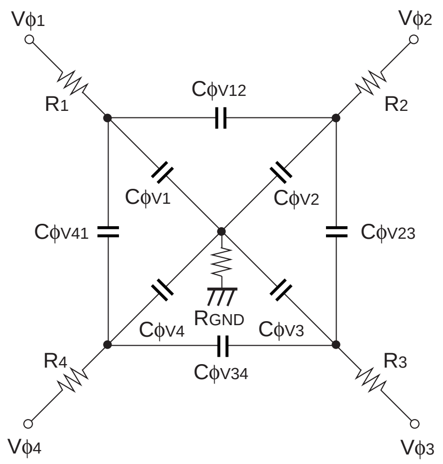
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.6	–9.0	–8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V_{\phi V}$	8.3	9.0	9.65	Vp-p	2	$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3} - V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} - V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.75	5.0	5.25	Vp-p	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage*1	V_{RGL}		*1		V	4	
	$V_{\phi RG}$	4.5	5.0	5.5	Vp-p	4	
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	23.0	24.0	25.0	Vp-p	5	

*1 Input the reset gate clock without applying a DC bias. In addition, the reset gate clock can also be driven with the following specifications.

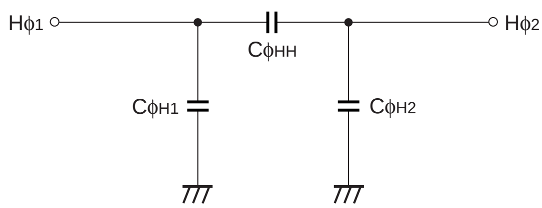
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0	0.2	V	4	
	$V_{\phi RG}$	8.5	9.0	9.5	Vp-p	4	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		3300		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		3300		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		820		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		330		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$		120		pF	
	$C\phi_{H2}$		91		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		47		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		11		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		680		pF	
Vertical transfer clock series resistor	R_1, R_3		75		Ω	
	R_2, R_4		82		Ω	
Vertical transfer clock ground resistor	R_{GND}		68		Ω	



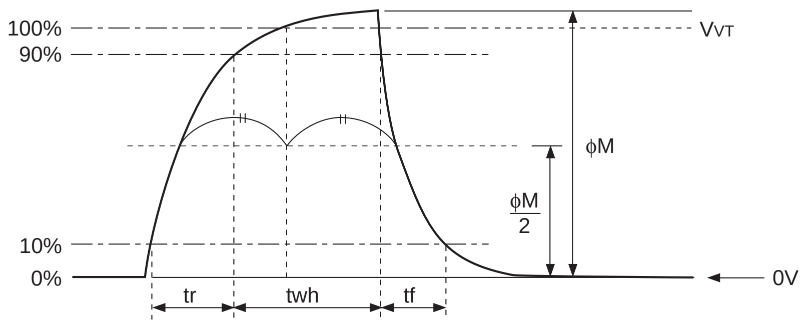
Vertical transfer clock equivalent circuit



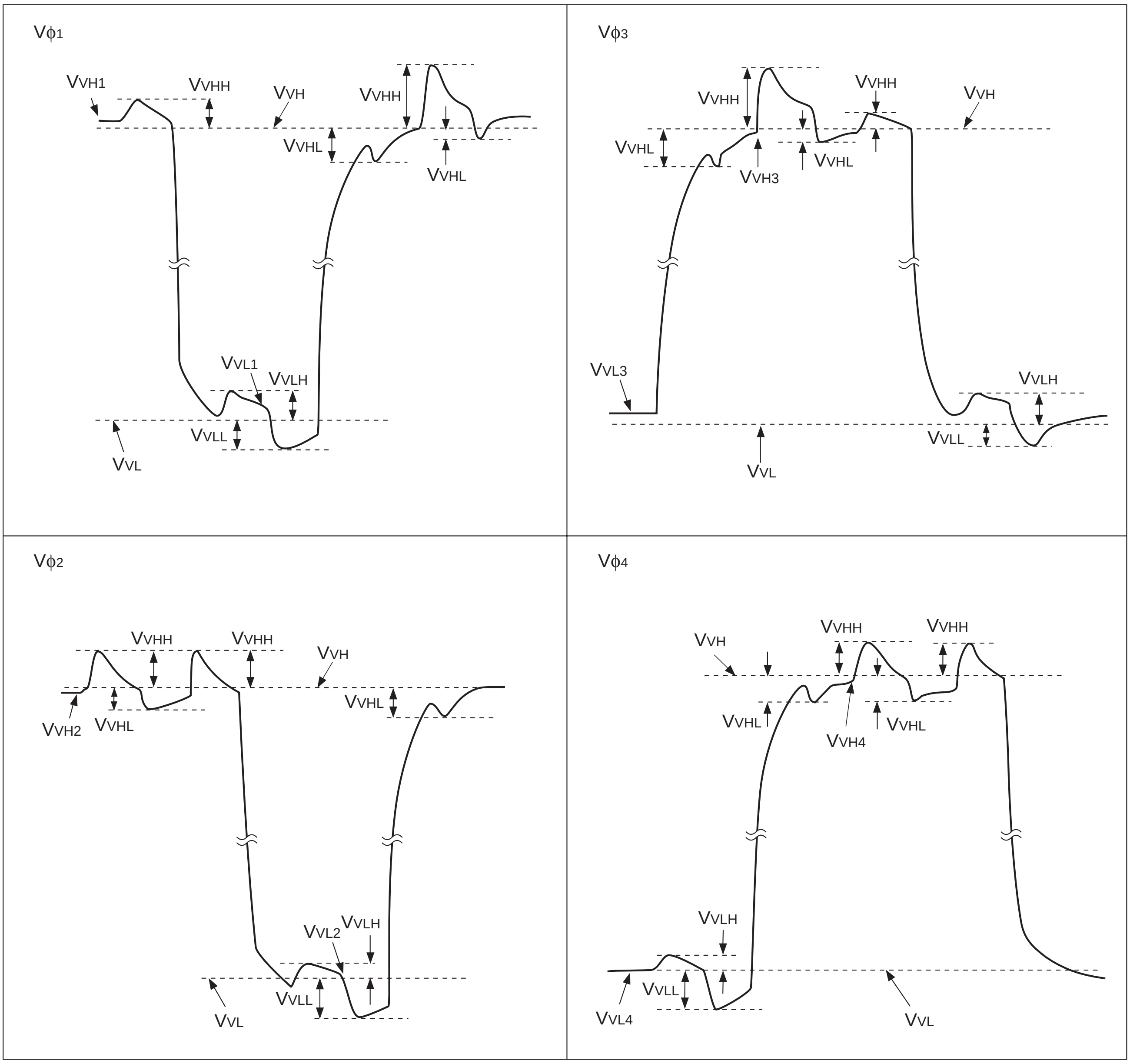
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

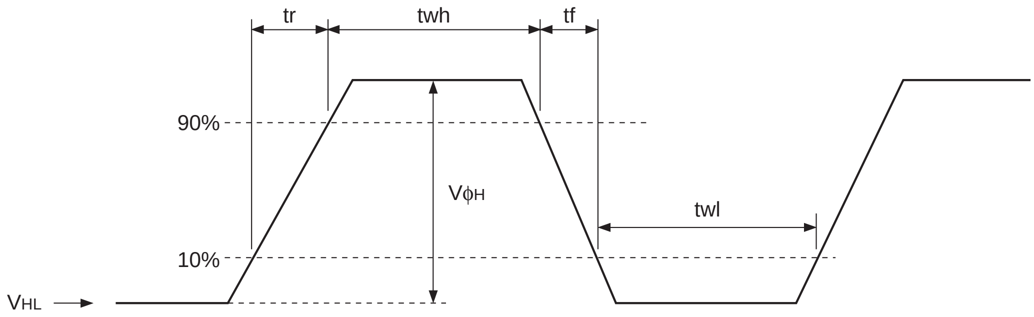


$V_{VH} = (V_{VH1} + V_{VH2})/2$

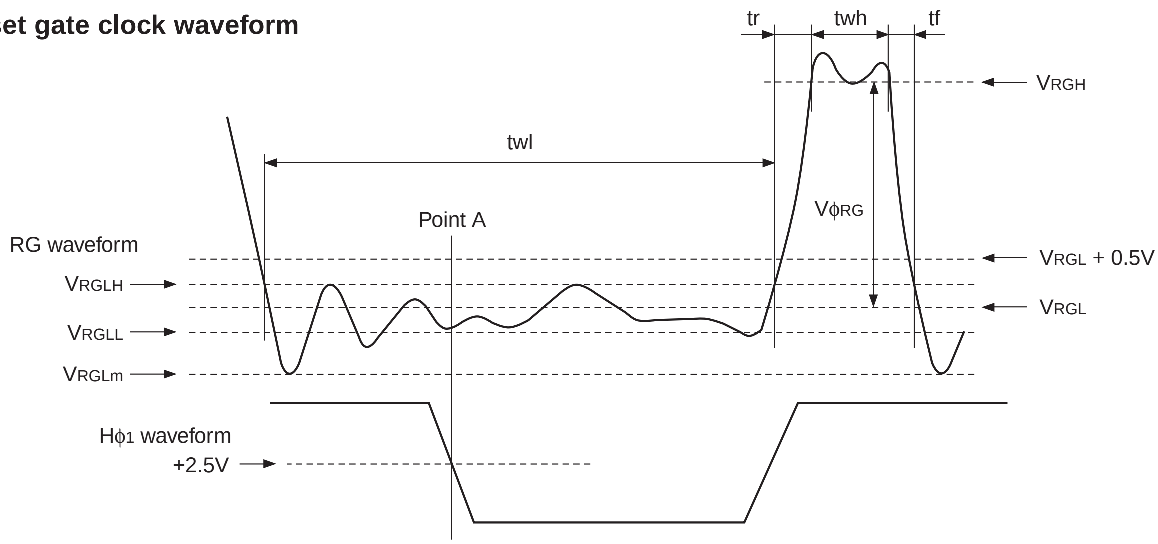
$V_{VL} = (V_{VL3} + V_{VL4})/2$

$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



(4) Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

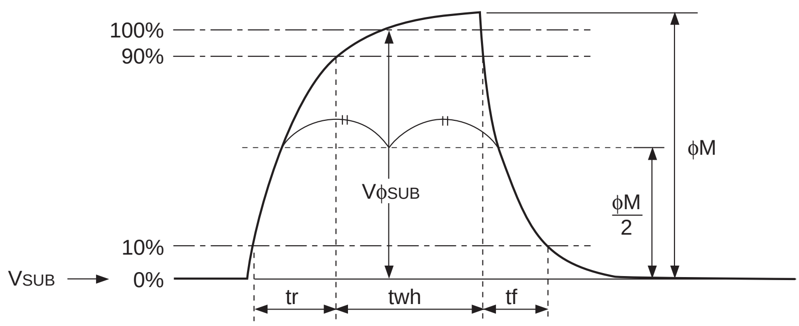
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

Assuming V_{RGH} is the minimum value during the period twh, then:

$V\phi_{RG} = V_{RGH} - V_{RGL}$

Negative overshoot level during the falling edge of RG is V_{RGLm}.

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5					0.5			0.5			μs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	*1
Horizontal transfer clock: During imaging	$H\phi$		20			20			15	19		15	19	ns	*2
Horizontal transfer clock: During parallel-serial conversion	$H\phi_1$		5.38						0.01			0.01		μs	
	$H\phi_2$					5.38			0.01			0.01		μs	
Reset gate clock	ϕRG	11	13			51			3			3		ns	
Substrate clock	ϕSUB	1.5	1.8							0.5			0.5	μs	When draining charge

*1 When vertical transfer clock driver CXD1267AN is used.

*2 tf ≥ tr – 2ns.

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	16	20		ns	*3

*3 The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity1	S1	1120	1400		mV	1	
Sensitivity2	S2	4500	5500		mV	2	
Saturation signal	Vsat	1000			mV	3	Ta = 60°C
Smear	Sm		–126	–115	dB	4	
Video signal shading	SH			20	%	5	Zone 0 and I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	7	Ta = 60°C
Flicker	F			2	%	8	
Lag	Lag			0.5	%	9	

Zone Definition of Video Signal Shading

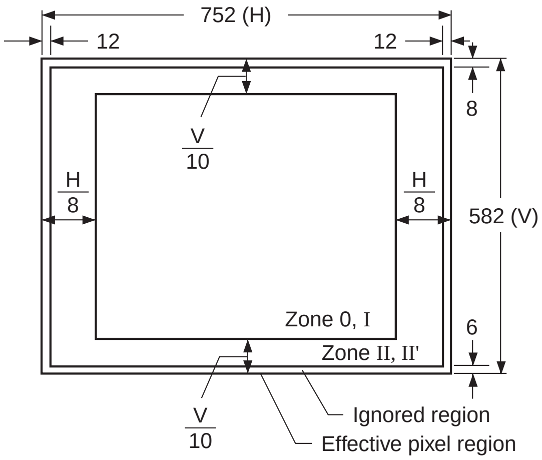


Image Sensor Characteristics Measurement Method

◎ Measurement conditions

1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions. (when used with substrate bias external adjustment, set the substrate voltage to the value indicated on the device.)

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of Y signal output or chroma signal output of the measurement system.

◎ Definition of standard imaging conditions

1) Standard imaging condition I:
Use a pattern box (luminance 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.4mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
This indicates the standard imaging condition I with the IR cut filter removed.

3) Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens and the luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm. (IR cut filter is not spplicable.)

1. Sensitivity1
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (V_{S1}) at the center of the screen and substitute the value into the following formula.

$$S1 = V_{S1} \times \frac{250}{50} \text{ [mV]}$$

2. Sensitivity2
Set to standard imaging condition II. After selecting the electronic shutter mode with a shutter speed of 1/1000s, measure the signal output (V_{S2}) at the center of the screen and substitute the value into the following formula.

$$S2 = V_{S2} \times \frac{1000}{50} \text{ [mV]}$$

3. Saturation signal
Set to standard imaging condition III. After adjusting the luminous intensity to 10 times the intensity with average value of the signal output, 200mV, measure the minimum value of the signal output.

4. Smear

Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of the signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value VSm [mV] of the signal output and substitute the value into the following formula.

$$Sm = 20 \times \log \left(\frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB] (1/10V method conversion value)}$$

5. Video signal shading

Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/200 \times 100 \text{ [\%]}$$

6. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading

After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

8. Flicker

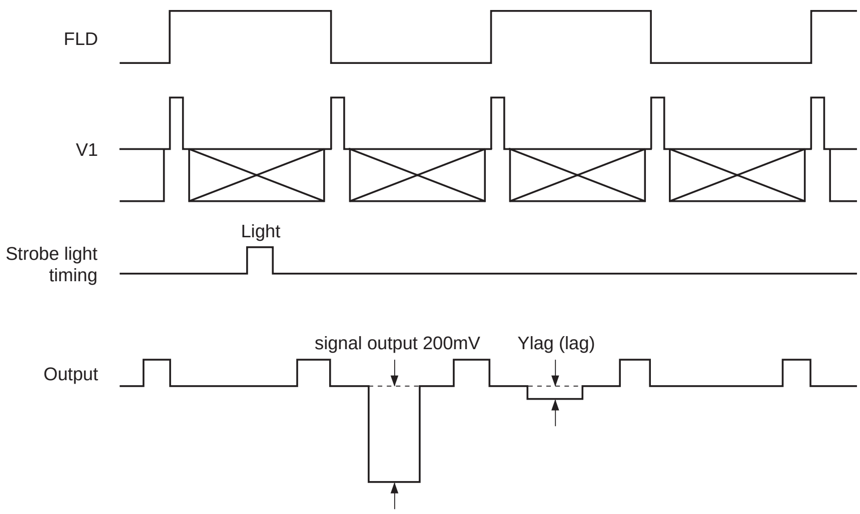
Set to standard imaging condition III. Adjust the luminous intensity so that the average value of the signal output is 200mV, and then measure the difference in the signal level between fields (ΔVf [mV]). Then substitute the value into the following formula.

$$Fy = (\Delta Vf/200) \times 100 \text{ [\%]}$$

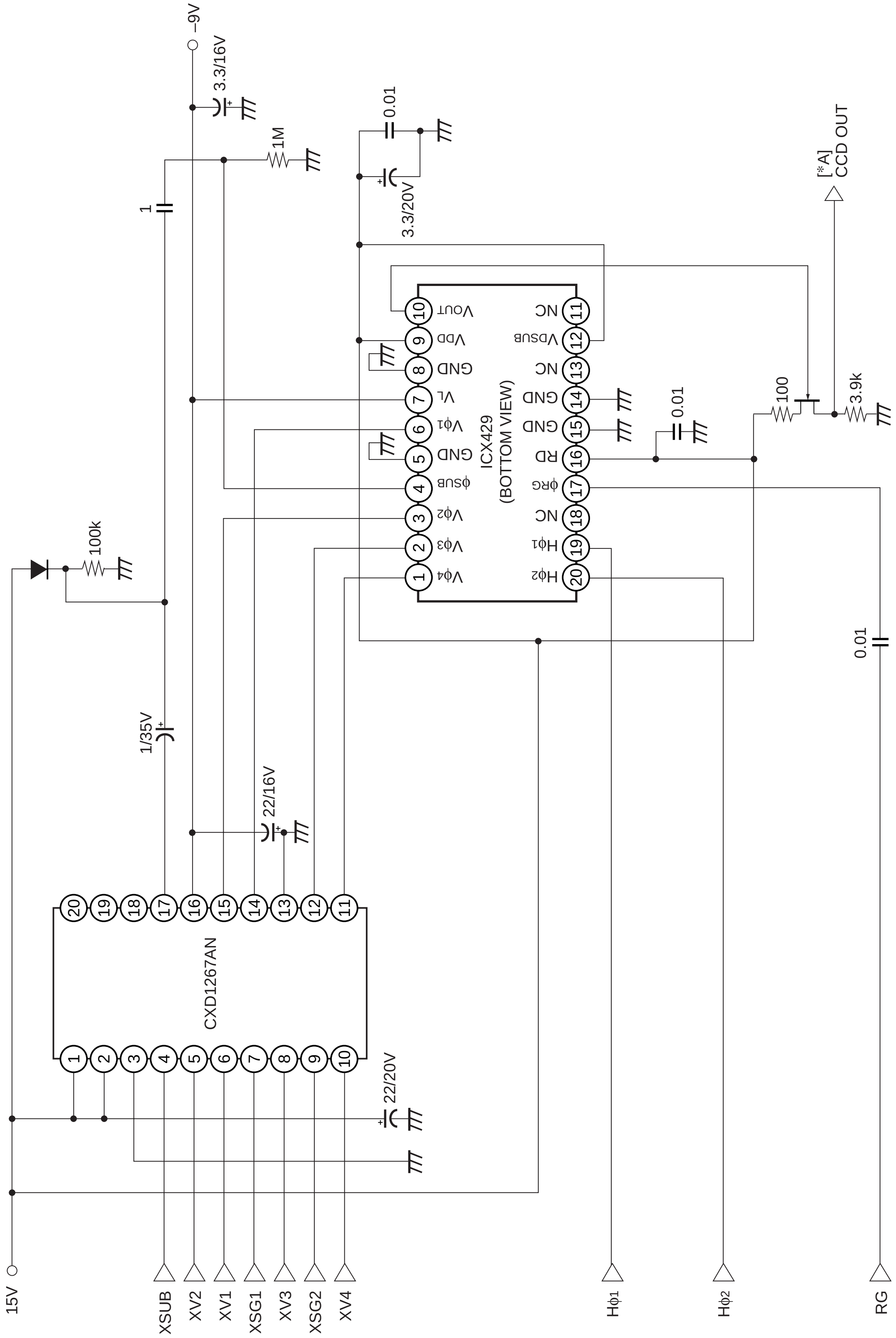
9. Lag

Adjust the signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

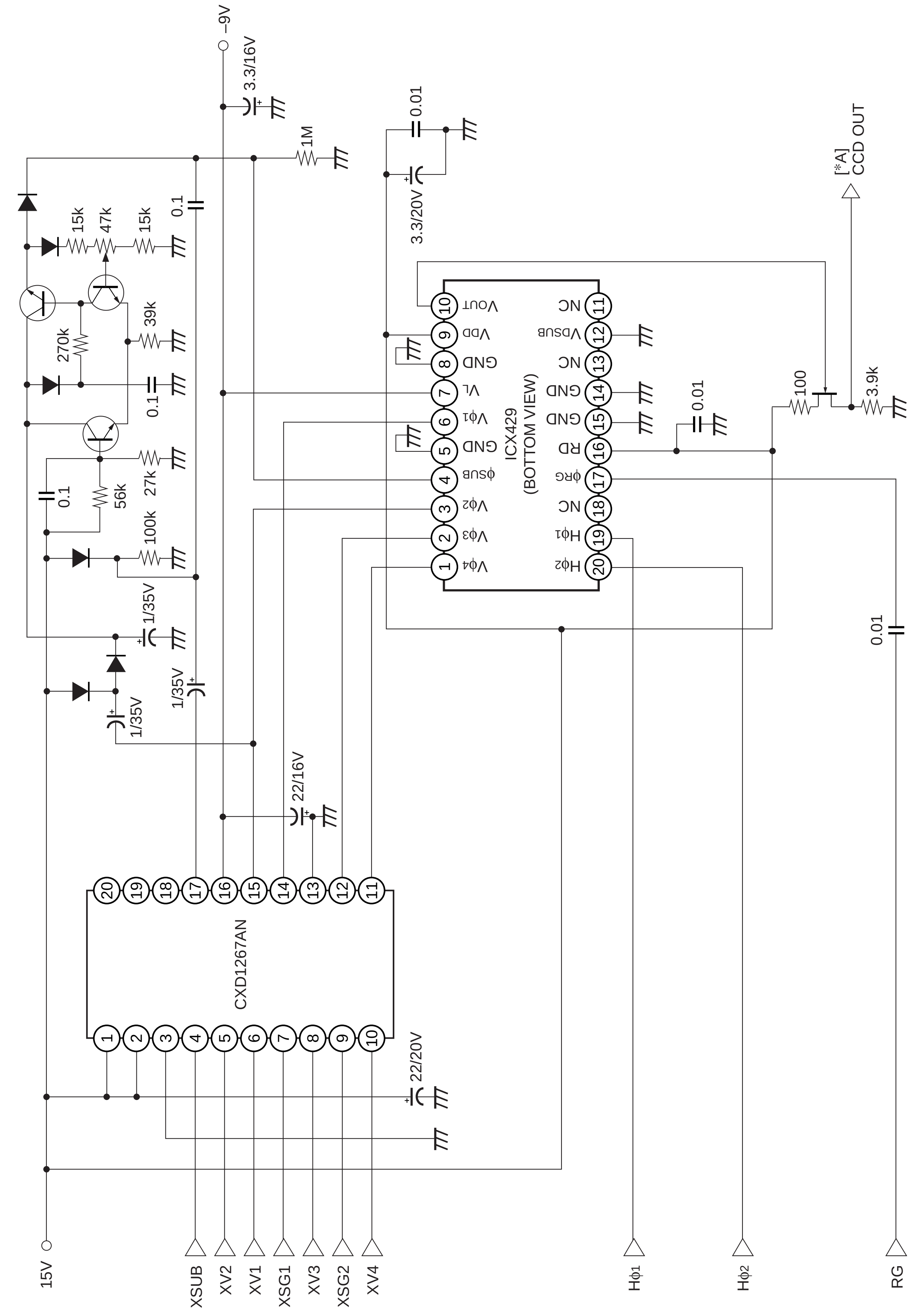
$$Lag = (Vlag/200) \times 100 \text{ [\%]}$$



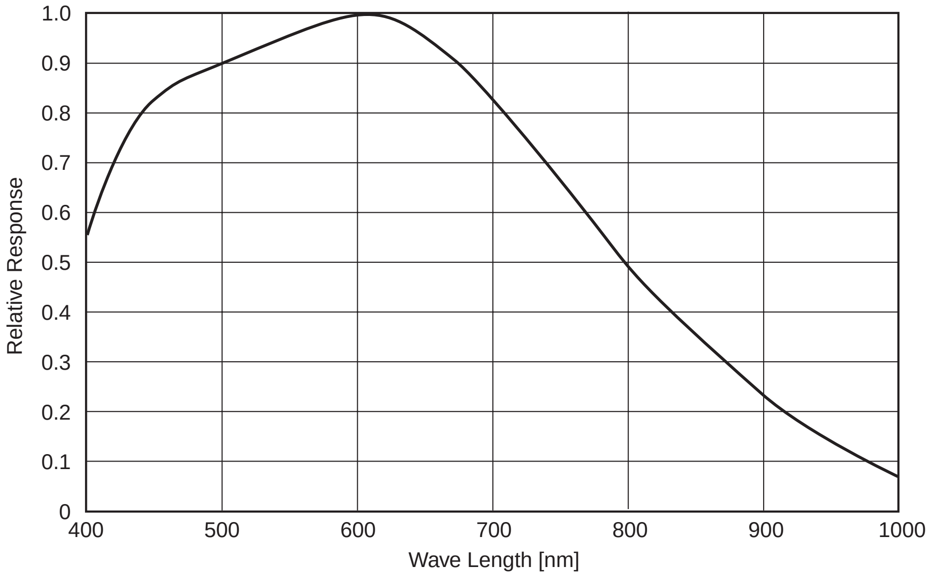
Drive Circuit 1 (substrate bias internal generation mode)



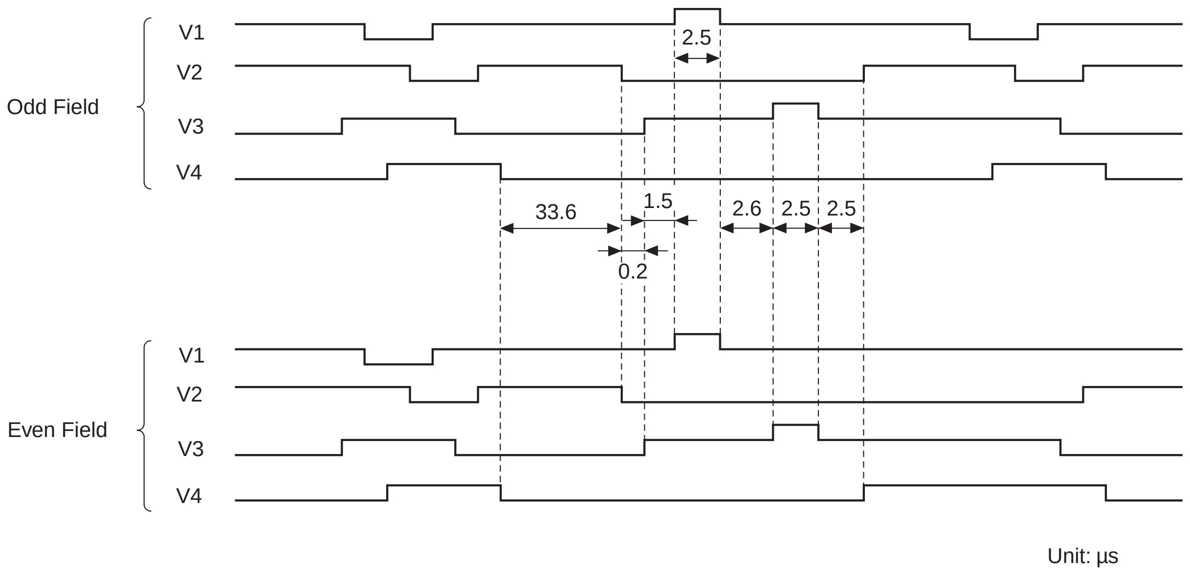
Drive Circuit 2 (substrate bias external adjustment mode)



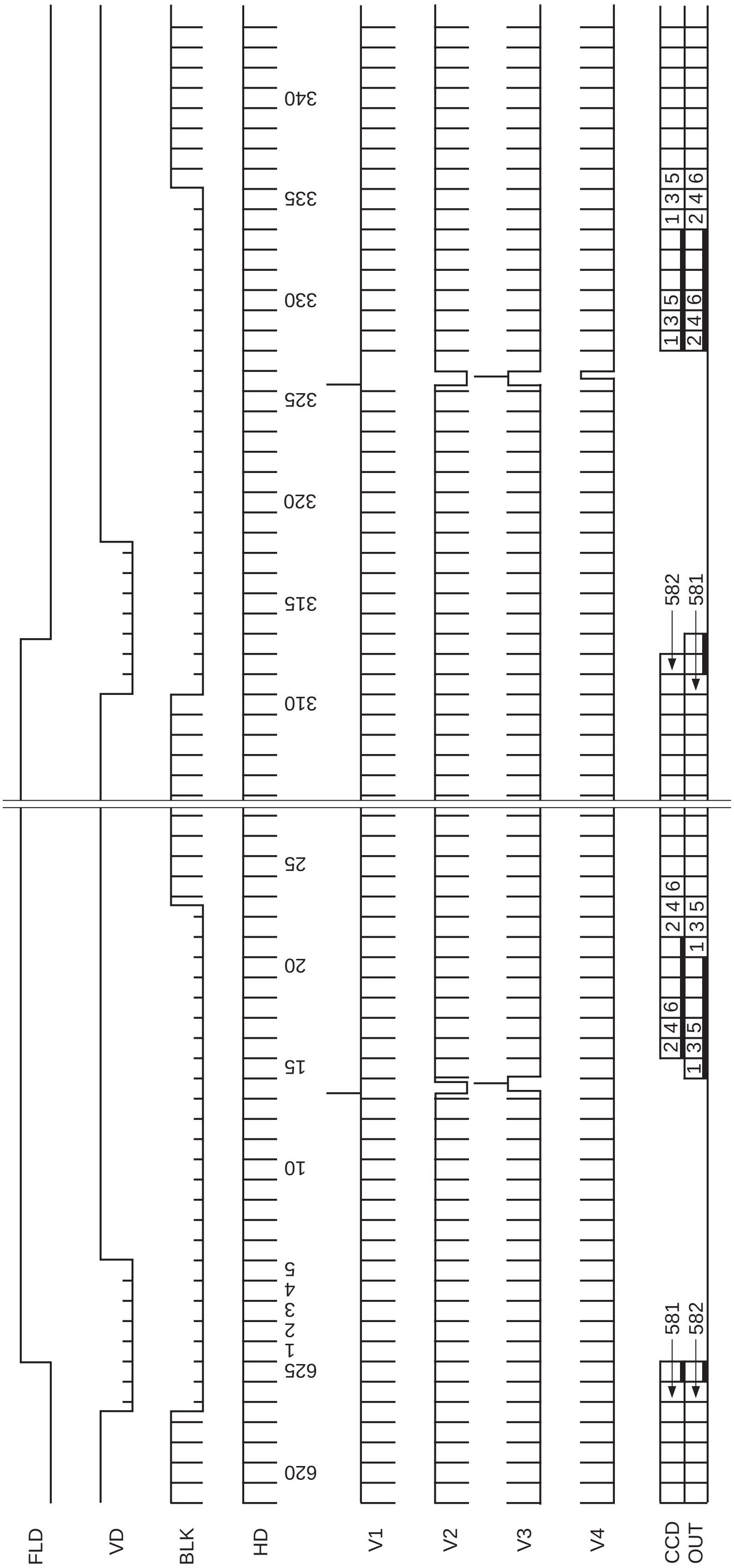
Spectral Sensitivity Characteristics (Excludes lens characteristics and light source characteristics)



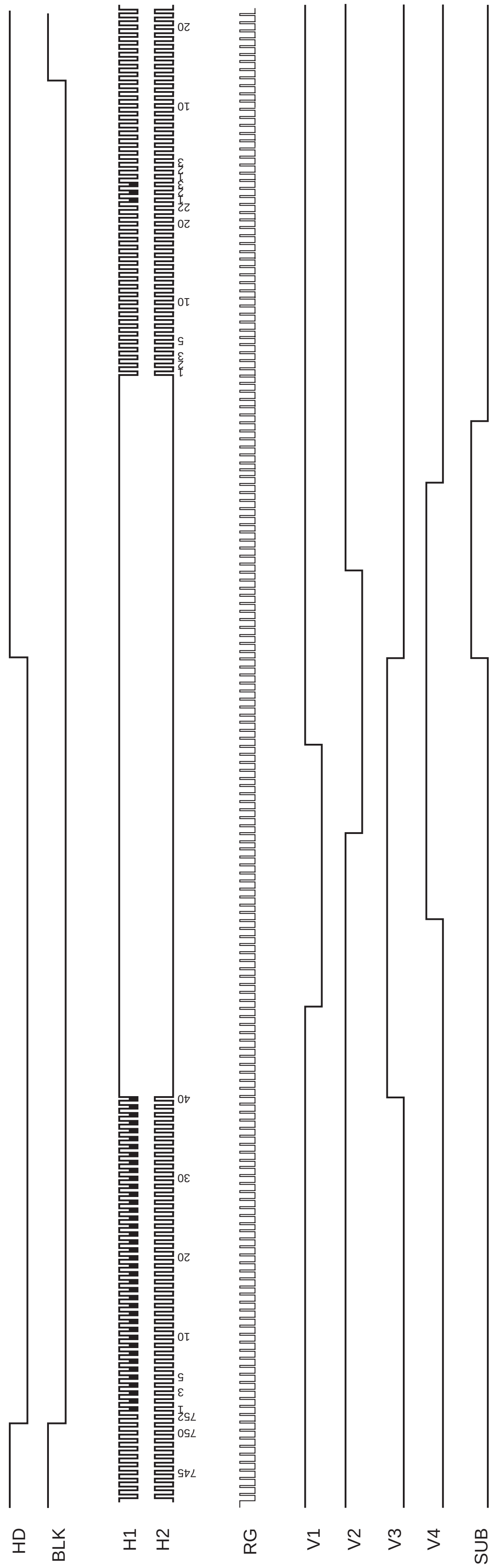
Sensor Readout Clock Timing Chart



Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



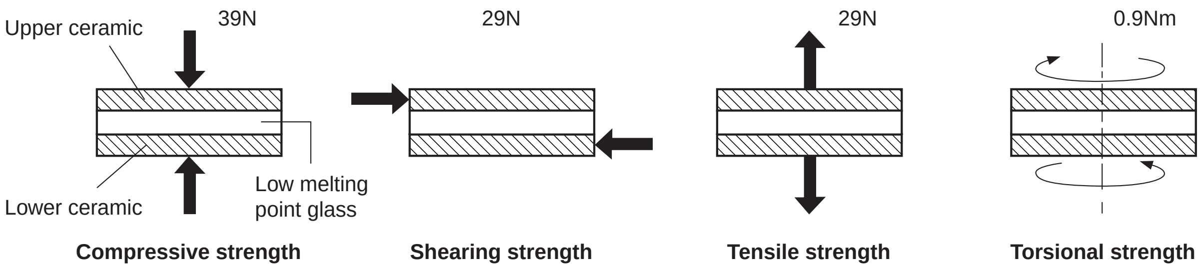
Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection
Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
a) Perform all assembly operations in a clean room (class 1000 or less).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portions. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.

d) The upper and lower ceramic are joined by low melting point glass. Therefore, care should be taken not to perform the following actions as this may cause cracks.

- Applying repeated bending stress to the outer leads.
- Heating the outer leads for an extended period with a soldering iron.
- Rapidly cooling or heating the package.
- Applying any load or impact to a limited portion of the low melting point glass using tweezers or other sharp tools.
- Prying at the upper or lower ceramic using the low melting point glass as a fulcrum.

Note that the same cautions also apply when removing soldered products from boards.

e) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others

a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

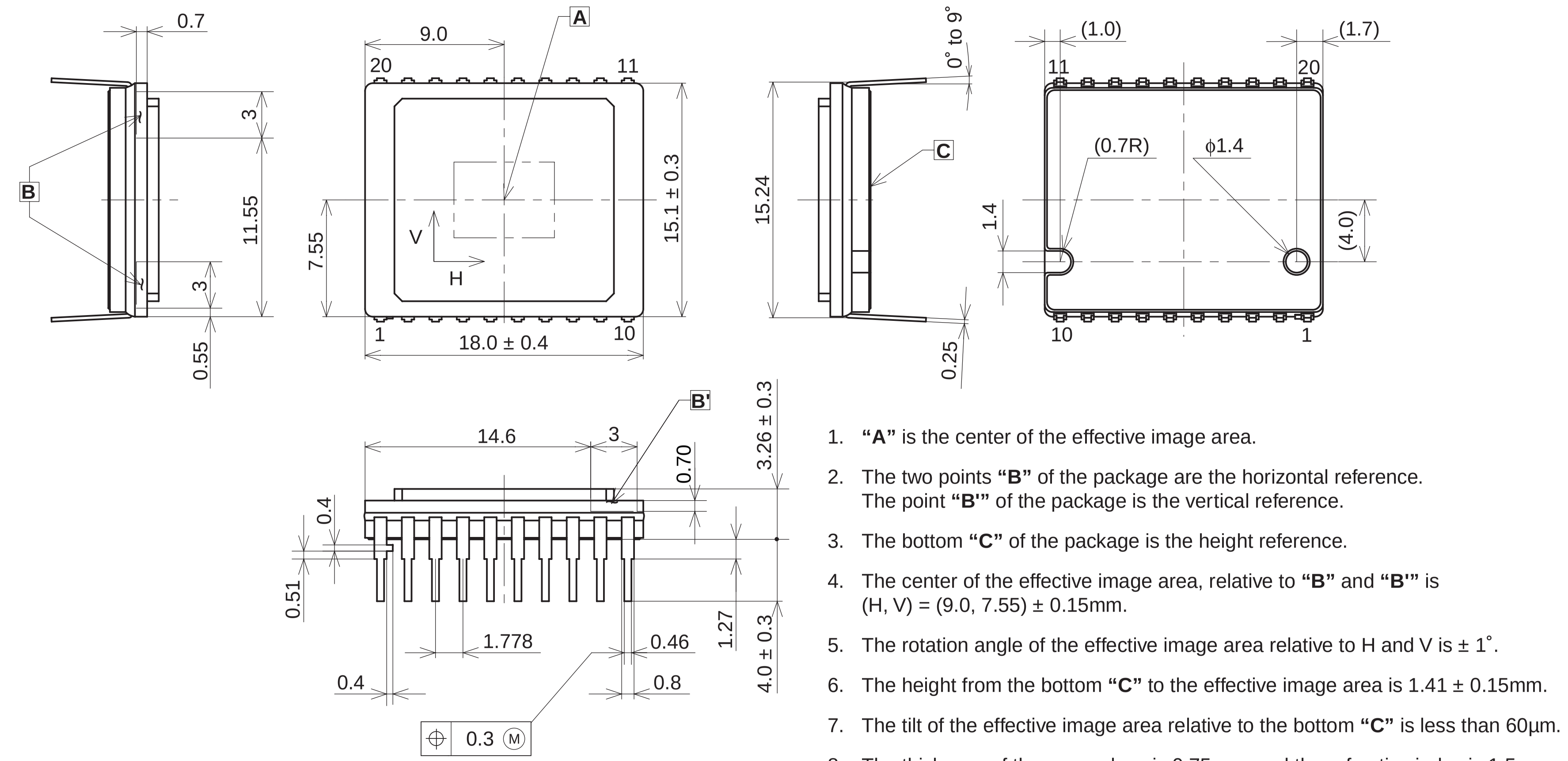
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

c) This CCD image sensor has sensitivity in the near infrared srea. Its focus may not match in the same condition under visible ligth / near infrared ligth bocause of aberration.

Package Outline

Unit: mm

20pin DIP (600mil)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package is the height reference.
4. The center of the effective image area, relative to **"B"** and **"B'"** is
   (H, V) = (9.0, 7.55) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 60µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch and the hole on the bottom must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.6g
DRAWING NUMBER	AS-B14-01(E)