



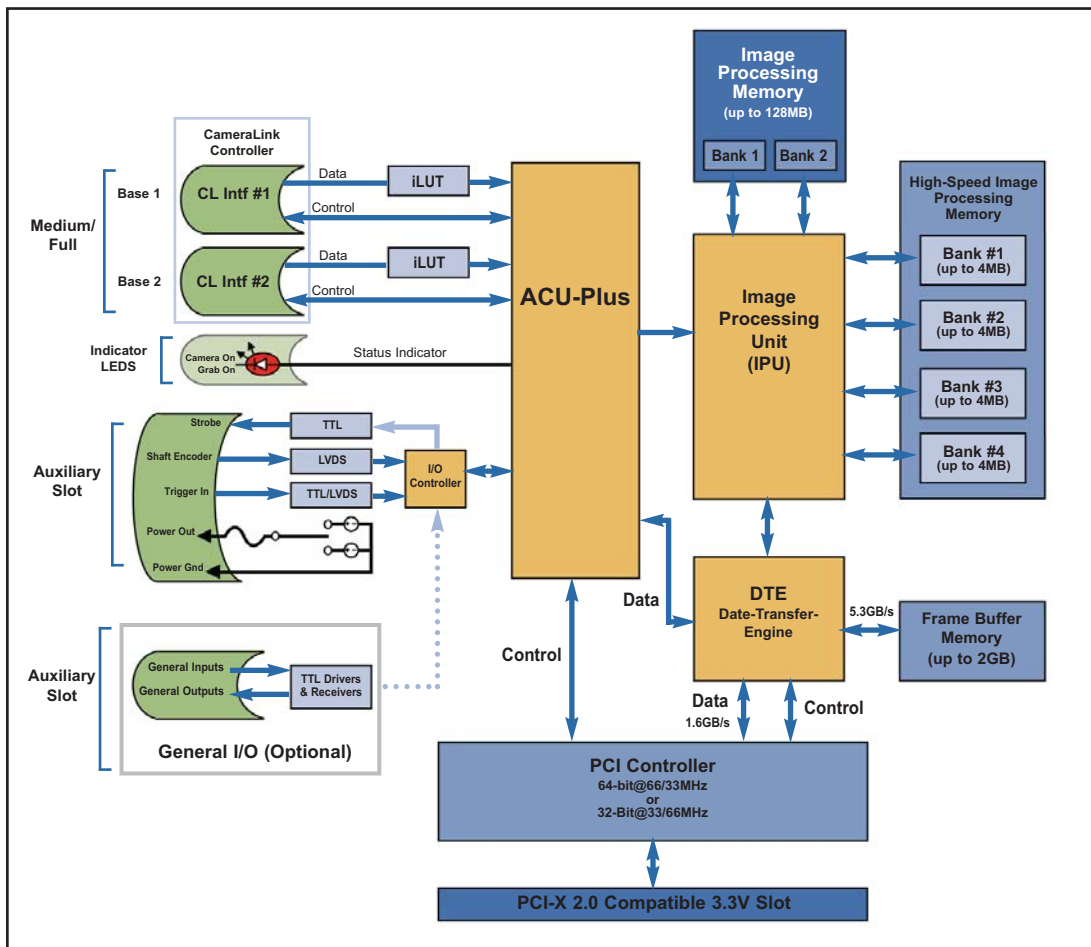
KEY FEATURES

- PCI-X vision processing board
- FPGA based for versatile and scalable application development
- Optimized memory architecture facilitates high-speed real-time processing
- High Speed RISC processor with SIMD architecture
- Image acquisition from area or linescan Camera Link ® cameras
- Trigger-to-Image Reliability ensures secure image capture

OVERVIEW

High speed **real-time** Vision processing

Coreco Imaging's Anaconda is at the vanguard of vision processing technology delivering dramatic improvements in image capture and data processing speeds while at the same time providing unprecedented board level application control. A powerful PCI-X image processing board, the Anaconda is specifically designed for real-time image acquisition, processing and analysis. It combines a high-speed image acquisition capability with a user programmable FPGA (Field Programmable Gate Array) and PowerPC™ CPU to deliver real-time image processing on a single slot platform. The Anaconda series allows users to combine their proprietary processing algorithms with finely tuned data control and event management functions to deliver high-performance embedded imaging. The Anaconda series is ideally suited for embedded vision applications where large amounts of image processing is required in fields such as diagnostic X-Ray, fluoroscopy, flat-panel inspection, and semiconductor wafer inspection.



Anaconda: Functional Block Diagram

Advanced Image Processing Development

At the heart of the Anaconda's functionality is the Image Processing Unit (IPU) allowing developers to implement their algorithms directly in hardware. There are three key elements within the IPU.

Configurable Hardware

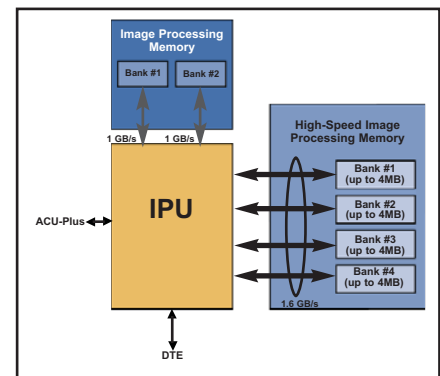
The IPU features a user configurable high density FPGA. Users with FPGA development expertise can leverage the Anaconda to bring high-performance solutions to market faster. The IPU comes bundled with user accessible FPGA code to manage data movement, bus arbitration, and other housekeeping functions. With all these critical and time consuming operations already taken care of, developers can concentrate on refining and optimizing their image processing algorithms to deliver innovative solutions to their respective markets. Secure and user controlled, the image processing functions can be developed on the IPU using standard FPGA development tools.

General-Purpose RISC Processor

The IPU's CPU combines a powerful 32 bit RISC processor with a single instruction multiple data (SIMD) architecture. The SIMD is ideal for signal and image processing applications. For accelerated performance, the CPU includes 4MB of L3 cache and 512KB of on-die cache for the CPU.

Optimized Memory Architecture

Anaconda's advanced memory architecture allows images to be accessed and processed concurrently; dramatically accelerating processing speeds by eliminating the amount of time the system is idle waiting for data to arrive. It does so by combining large amounts of physical memory with high-speed multiple independent access buses. The Anaconda delivers a cost effective solution for very complex processing applications by combining various types of memory. With reduced data sharing and supervisory control for other sub-sections on the board, the IPU can perform image processing and analysis autonomously, delivering highly optimized and efficient solutions for real-time image processing.



Anaconda: Memory Architecture

Specifications*

Board	Full length PCI-X Rev. 1.0 compliant card
Acquisition	<p>Acquisition rates up to 85MHZ Horizontal Size (min/max): 8 byte/256KB Vertical Size (min/max): Linescan cameras: 1 line to infinite length frames/variable length frames with start/stop trigger Area scan cameras: 1 line to 16 million One 1024 x 1024 or 1024 x 256 input lookup table Single slot solution supports 1 Full, 1 Medium or 1 Base Camera Link camera Interfaces to digital area scan or linescan color or monochrome cameras Pixel Formats Monochrome 8, 10, 12, 14, 16, or 36-bit/RGB Supports standard multi-tap Camera Link configurations:</p>
Full Camera Link	<p>One Full camera: 8 x 8-bit, or One Medium camera: 4 x 8-bit, 4 x 10-bit, 4 x 12-bit, 1 x 30-bit/RGB and 1 x 36-bit, or One Base cameras: 3 x 8-bit, 2 x 10-bit, 2 x 12-bit, 1 x 14-bit, 1 x 16-bit, and 1 x 24-bit/RGB</p>
Memory	<p>Frame Buffer: up to 2GB (256MB standard) Image Processing: 128MB High-Speed Image Processing: 4x MB</p>
Transfer	<p>Transfers Real-time transfers to system memory: PCI-X bus: 32 bit @ 33MHz PCI-X bus: 64 bit @ 66MHz PCI-X bus: 64 bit @ 100/133MHz On-the-fly tap adjustments for multiple tap area scan and linescan cameras</p>
Processing	<p>FPGA – Xilinx Virtex-Pro™ XC2VP20¹ Embedded CPU – Motorola PowerPC: PowerPC MPC7457</p>
Controls	<p>Comprehensive event notification includes start/end-of-frame, sequence or N-line events Two opto-isolated TTL/LVDS trigger input independently programmable as active high or low (edge or level trigger) One strobe TTL output One PC independent serial communication port provides seamless interface to MS Windows applications Quadrature (AB) shaft-encoder inputs for external web synchronization Up to 12 interrupt driven I/Os permit external event synchronization</p>
Dimensions	12.283" (31.20cm) Length x 4.20" (10.7cm) Height
Temperature	0° C (32° F) to 55° C (131° F)
Relative Humidity	Up to 95% (non-condensing)
Markings	<p>FCC class B – Pending CE class B – Pending</p>

* Revision date: November 2004

Notes:

1. Contact Coreco Imaging for other supported devices

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