F-145B / F-145C AVT Dolphin

Manual

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ALLIED
Vision Technologies

Contents

Before operation

We place the highest demands for quality on our cameras.
This manual should help you with the installation and setting up the camera for use.
Please read through the manual carefully before operating the camera.

Legal notice

For customers in the U.S.A.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. You are cautioned that any changes or modifications not expressly approved in this manual could void your authority to operate this equipment. The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC Rules.

For customers in Canada

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

Pour utilisateurs au Canada

Cet appareil est conforme aux normes classe A pour bruits radioélectriques, spécifiées dans le Règlement sur le brouillage radioélectrique.

Life support Applications
These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Allied customers using or selling these products for use in such applications do so at their own risk und agree to fully indemnify Allied for any damages resulting from such improper use or sale.

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Conventions used in this manual

In order to give this manual in an easily understood layout and to emphasize important information, the following typographical styles and symbols are used:

Styles

Style	Function	Example
Courier	Programs, inputs, etc.	"Input"
upper case	Register	REGISTER
italics	Modes, fields	*Mode*
parentheses and/or blue	Links	(Link)
	Write register	
	Read register	

Symbols

ⓘ This symbol highlights important instructions that you should make sure to follow if you want to avoid malfunctions.

1 Safety instructions

There are no switches or parts inside of the camera that require adjustment. The guarantee becomes invalid upon opening the camera casing.

1.1 Environmental conditions

Ambient temperature:

when camera in use	- 5° C ... + 45° C
when being stored	- 10° C ... + 60° C

relative humidity no condensed water	20% ... 80%

2 Device type and range of application

The AVT F-145 is an IEEE 1394 SXGA+ camera. Equipped with a 1.45 megapixel 2/3" progressive CCD sensor, it features a modular concept, large internal storage and a variety of intelligent preprocessing options.

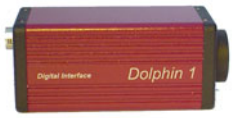
Among these are real time shading correction and up to 63 user-defined lookup tables.

The AVT DOLPHIN F-145 is also suitable for all imaginable image processing tasks, especially due to its high speed of up to 15 fps.
It can be easily integrated into any existing system environment through a flexible and high-performance API. The API is available as an option.

The camera is available in both a B/W (F-145B) and color (F-145C) models. The operation of both models is described in this documentation.

2.1 System components

The following system components are included with delivery:



AVT Dolphin

4.5m 1394 industrial cable

Optional:

AT – ST tripod adaptor

BG39 IR cut filter (650 nm)

Driver and documentation

To demonstrate the properties of the camera, all examples in this manual are based on the "FirePackage" OHCI API software and the "FireView" application.

This can be obtained from Allied Vision Technologies. A free demo version of "FireView" is available for download at www.alliedvisiontec.com.

Of course the camera also works with all IIDC (formerly DCAM) compatible IEEE 1394 programs and image processing libraries.

AVT offers different lenses from a variety of manufacturers. The following table lists selected image formats depending on distance and the focal width of the lens.

Focal Width F-145	Distance = 0.5m	Distance = 1m
4.8 mm	0.7 m x 0.93 m	1.4 m x 1.86 m
8 mm	0.4 m x 0.53 m	0.8 m x 1.06 m
12 mm	0.27 m x 0.36 m	0.54 m x 0.72 m
16 mm	0.2 m x 0.27 m	0.4 m x 0.54 m
25 mm	12.5 cm x 16.625 cm	25 cm x 33.25 cm
35 mm	8.8 cm x 11.7c m	17.6 cm x 23.4 cm
50 mm	6 cm x 7.98 cm	12 cm x 15.96 cm

3 Specifications

3.1 F-145B

Specification	
Image device	2/3 Type progressive scan b/w SONY IT CCD
Effective Picture Elements	1392 (H) x 1040 (V)
Lens Mount	C-Mount
Picture Sizes	640 x 480 pixels (Format_0; Mode_5 and _6) 800 x 600 pixels (Format_1; Mode_2 and _6) 1024 x 768 ((Format_1; Mode_5 and _7) 1280 x 960 (Format_2; Mode_2 and _6) 1392 x 1040 (Format_7; Mode_0) 696 x 1040 (Format_7; Mode_1) horizontal binning 1392 x 520 (Format_7; Mode_2) vertical binning 696 x 520 (Format_7; Mode_3) h+v binning
Cell Size	6.45 µm x 6.45 µm (12.9 µm x 12.9 µm in h+v binning)
ADC	12 Bit
Data Path	8 Bit or 10 Bit
Frame rates	3.75 Hz; 7.5 Hz; 15 Hz; External Trigger Shutter
Gain Control	Manual 0 – 30 dB (0.035 dB/step)
Shutter Speed	1-4095 x Timebase Timebase: 1, 2, 5, 20, 50, 100, 200, 500, 1000µs
External Trigger	Trigger Mode_0
Shutter	Advanced feature: Image Transfer by command
Internal Memory	Up to 16 frames
# Look Up Tables	Up to 63, user programmable (12 Bit -> 10/8 Bit); Gamma (0.45)
Smart Functions	Real Time Shading correction; Image Sequencing, three configurable inputs, three configurable outputs
Transfer Rate	400 Mb/s
Digital Interface	IEEE 1394 IIDC v. 1.3
Power Requirements	DC 8V – 36V via IEEE 1394 cable or 12-pin HIROSE
Power Consumption	Less than 3.5 Watt (at 12V DC)
Dimensions	115 mm x 45 mm x 45 mm (L x W x H); w/o tripod and lens
Mass	230 gr (without lens)
Operating Temperature	+ 5 / - 45 ° Celsius
Storage Temperature	-10 / - 60 ° Celsius
Regulations	EN 55022; EN 61000-6-2; FCC Class A
Options	Removable IR-Cut-Filter, Host Adapter Card, API (FirePackage)

The design and specifications for the product described may change without notice.

3.2 F-145C

Specification	
Image device	2/3 Type progressive scan Color SONY IT CCD
Effective Picture Elements	1392 (H) x 1040 (V)
Lens Mount	C-Mount
Picture Sizes	320 x240 pixels (Format_0; Mode_1) 640 x 480 pixels (Format_0; Mode_2, 3, 5 and _6) 800 x 600 pixels (Format_1; Mode_0, 2 and _6) 1024 x 768 ((Format_1; Mode3, 5 and _7) 1280 x 960 (Format_2; Mode0, 2 and _6) 1392 x 1040 (Format_7; Mode_1) Mono8 ; Mono16 1392 x 1038 (Format_7 ; Mode_0) YUV4 :2 :2 ; YUV4 :1 :1
Cell Size	6.45 µm x 6.45 µm
ADC	12 Bit
Data Path	8 Bit or 10 Bit
Frame rates	1.875 Hz; 3.75 Hz; 7.5 Hz; 15 Hz; External Trigger Shutter
Gain Control	Manual 0 – 24 dB (0.035 dB/step)
Shutter Speed	1-4095 x Timebase Timebase: 1, 2, 5, 20, 50, 100, 200, 500, 1000µs
External Trigger Shutter	Trigger Mode_0 Advanced feature: Image Transfer by command
Internal Memory	Up to 16 frames
# Look Up Tables	Up to 63, user programmable (12 Bit -> 10/8 Bit); Gamma (0.45)
Smart Functions	Image Sequencing, Color Conversion, Color Correction, three configurable inputs, three configurable outputs
Transfer Rate	400 Mb/s
Digital Interface	IEEE 1394 IIDC v. 1.3
Power Requirements	DC 8V – 36V via IEEE 1394 cable or 12-pin HIROSE
Power Consumption	Less than 3.5 Watt (at 12V DC)
Dimensions	115 mm x 45 mm x 45 mm (L x W x H); w/o tripod and lens
Mass	230 gr (without lens)
Operating Temperature	+ 5 - 45 ° Celsius
Storage Temperature	-10 - 60 ° Celsius
Regulations	EN 55022; EN 61000-6-2; FCC Class A
Options	Host Adapter Card, API (FirePackage)

The design and specifications for the product described may change without notice.

3.3 Spectral sensitivity

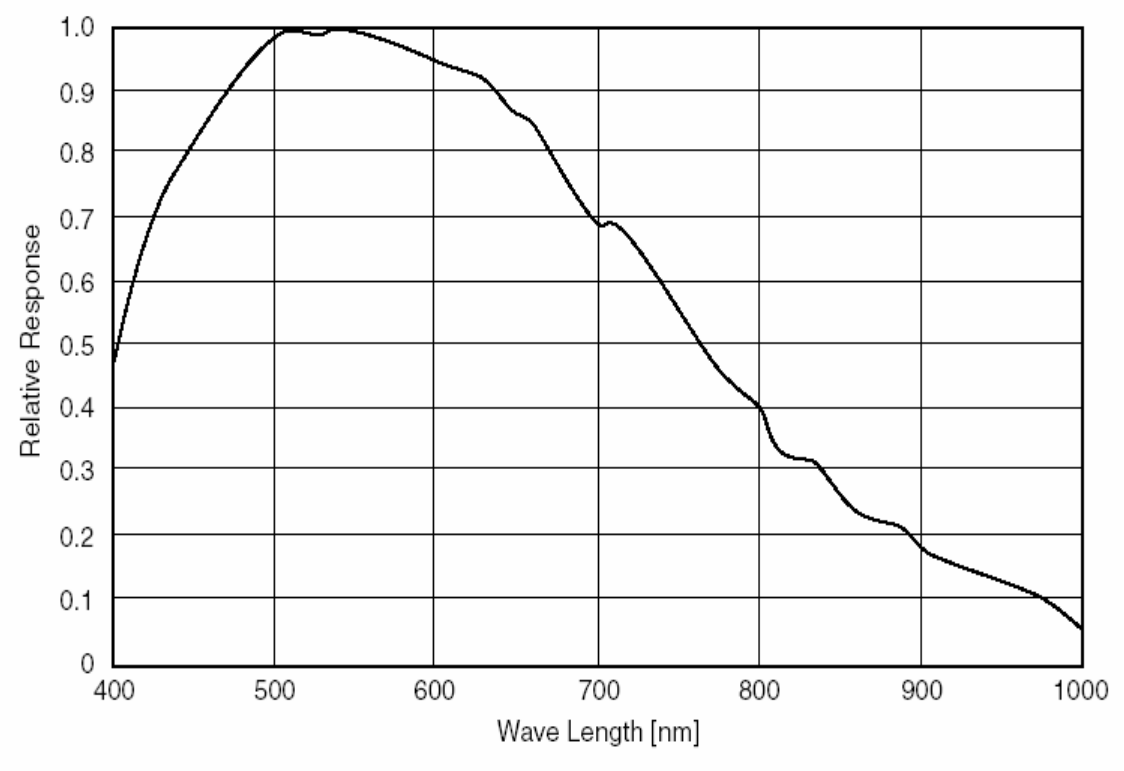


Figure 1 Spectral sensitivity F-145B without cut filter and without optics.

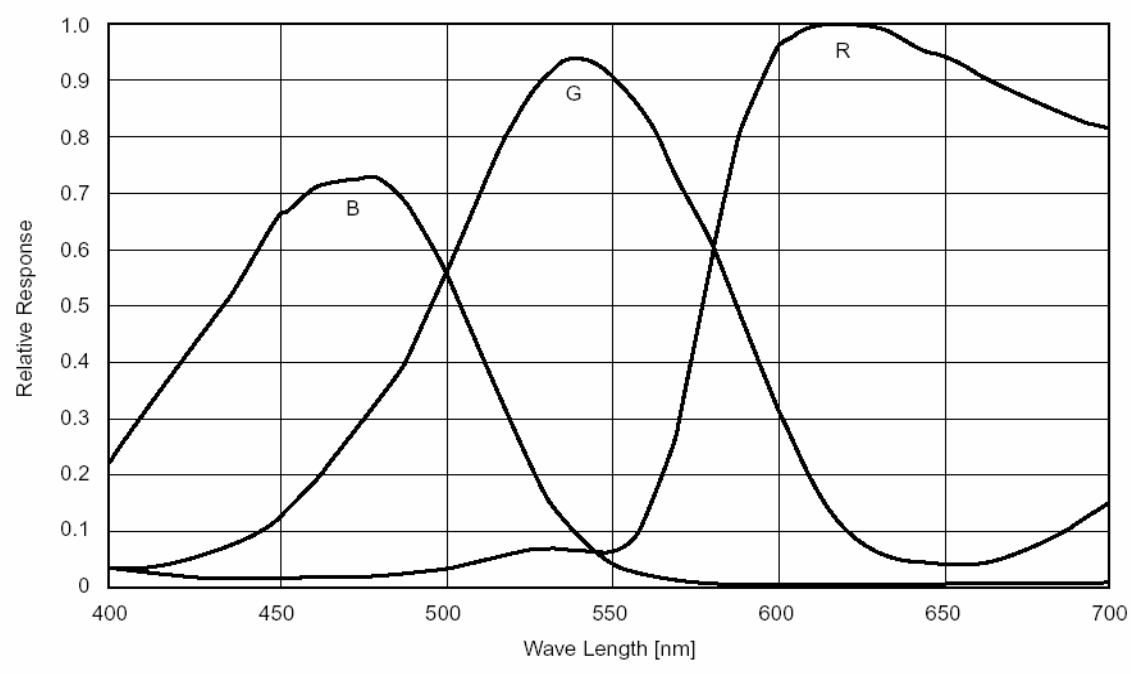


Figure 2 Spectral sensitivity F-145C without cut filter and without optics.

4 Quick start

To hook up an IEEE-1394 camera you need a PC with an IEEE-1394 port and appropriate software. The port is already present in many PCs and laptops. Should this not be the case, you can upgrade by installing one or more IEEE-1394 ports in the form of a card for the PCI slot or as a PC card (PCMCIA) for the PC card slot. AVT offers a range of adaptors for different requirements.

After starting the operating system the plug and play mechanism on the PC should recognize the new hardware and prompt you to install the IEEE-1394 driver from Microsoft. We nevertheless recommend installing the driver from Intek. This requires a FireWire adapter with a Texas Instruments PCI Lynx chip or a compatible OHCI chip.
The exact description for installation routines can be found in the “FireView” software manual.

The driver works in conjunction with the “Viewer” program. This enables quick and easy access to all integrated IEEE-1394 ports and all attached IEEE-1394 cameras.

After using the drop down list to choose a matching card, all available cameras for this card are displayed in the list below.

Select a camera and connect to this camera by clicking on the *Connect button*. The subsequent dialog offers the option of setting all available video formats and displays the frame in a corresponding window.

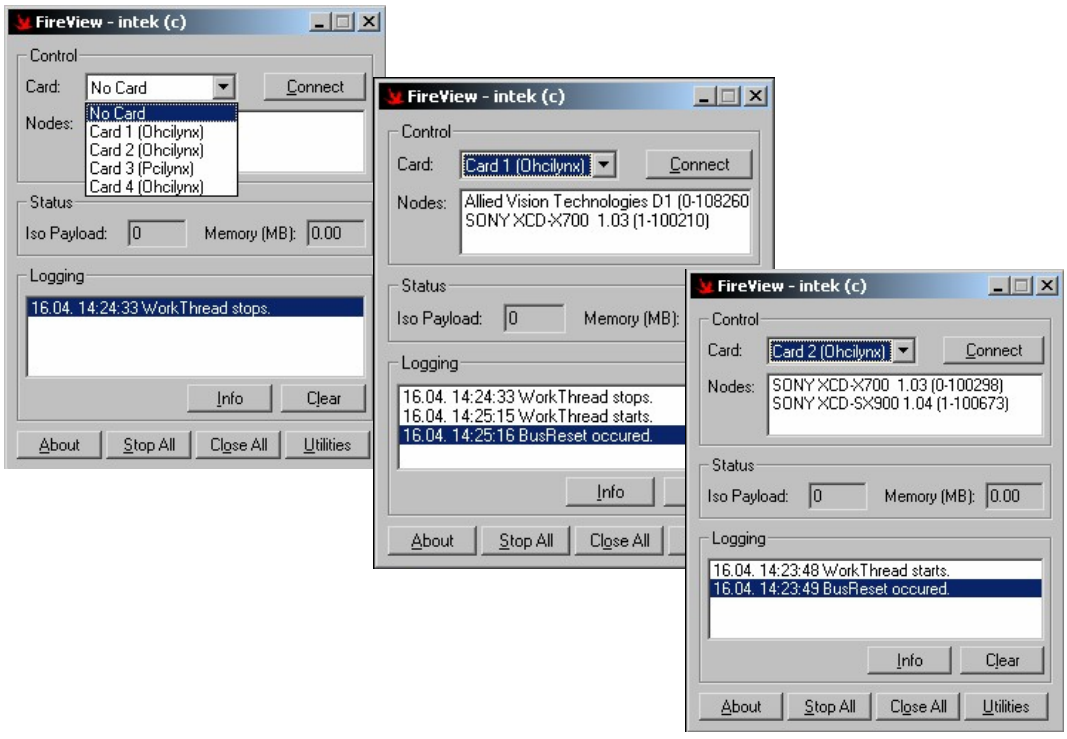


Figure 3 “FireView” program

In the *Live Control* dialog box you can make the settings for the standard registers according to the IIDC specification, e.g. exposure time or gain.

Direct access to the register level, e.g. to activate the advanced features of the camera, (see Advanced Feature Inquiry) is done via the *Directcontrol* dialog box.

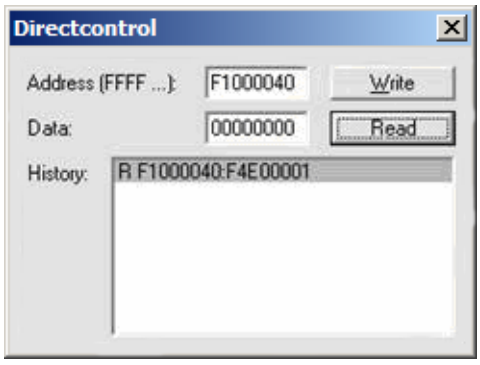


Figure 4 Directcontrol

5 Camera dimensions

Body size	(normal model)	115 x 45 x 45
	(offset lens)	140 x 62 x 45
Weight		225g

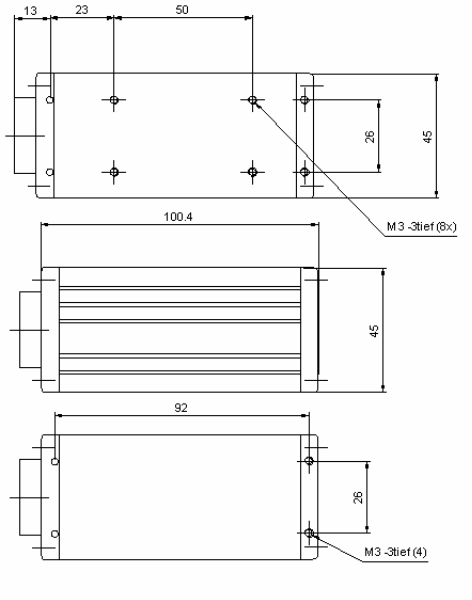


Figure 5 normal body

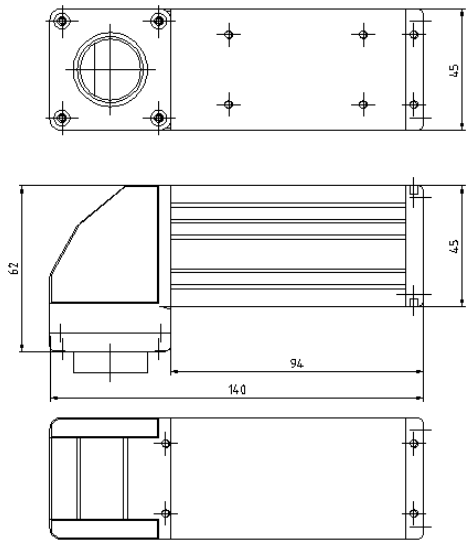


Figure 6 body with offset lens

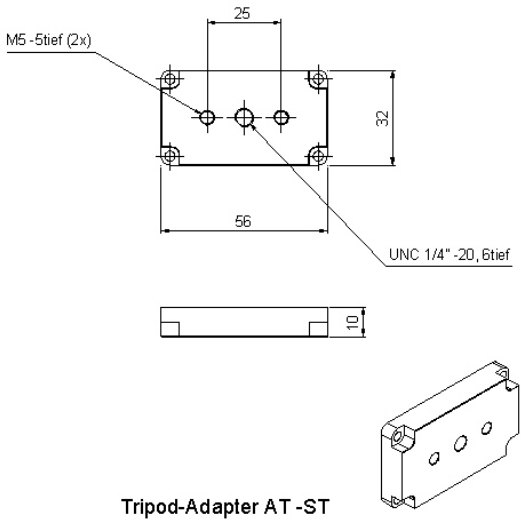


Figure 7 Optional tripod adapter

6 Camera interfaces

In addition to the status LEDs, both jacks are located on the back of the camera. The HiRose jack provides different control inputs and outputs The IEEE-1394 jack with lock-in mechanism provides access to the IEEE-1394 bus and thus makes it possible to control the camera and output frames.

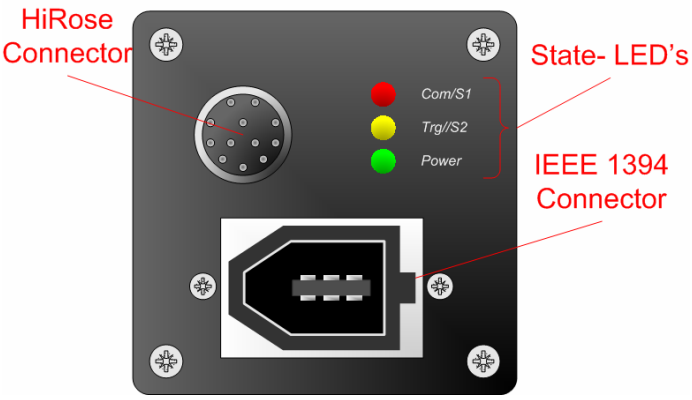
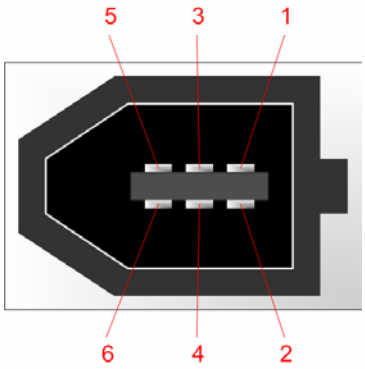


Figure 8 Camera interfaces

6.1 IEEE-1394 port pin assignment

The IEEE-1394 plug is suitable for industrial use and has the following pin assignment as per specification:



Pin	Signal	Pin	Signal
1	Cable Power	4	TPB+
2	Cable GND	5	TPA-
3	TPB-	6	TPA+

Figure 9 IEEE 1394 plug (view of plug)

6.2 HiRose jack pin assignment

The HiRose plug is also suitable for industrial use and in addition to providing access to the inputs and outputs on the camera, connects the camera to a power supply.

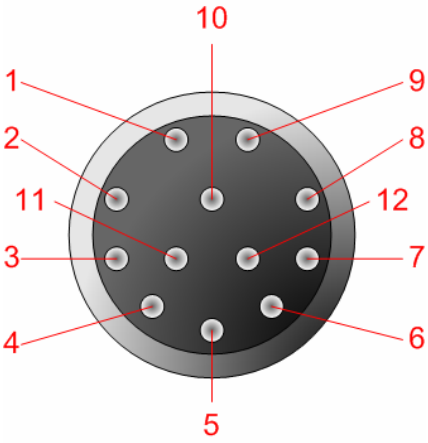


Figure 10 HiRose plug (view of contacts)

Pin	Signal	Use	Pin	Signal	Use
1	External GND		7	GPInput GND	
2	External Power	8-36 V DC	8	RS232 RxD	
3	GPInput 3	TTL	9	RS232 TxD	
4	GPInput 1 (default Trigger)	TTL, Edge, progr.	10	GPOutput GND	
5	GPOutput 3	Open collector	11	GPInput 2	TTL
6	GP Output 1 (default IntEna)	Open collector	12	GPOutput 2	Open collector

6.3 Status LEDs

6.3.1 On LED

The power LED indicates that the camera is being supplied with sufficient voltage and is generally ready for operation.

6.3.2 LEDs 1 and 2

The following states are displayed via the LEDs:

Com/S1	asynchronous and isochronous data transmission active (indicated asynchronously to transmission over the 1394 bus)
Trg/S2	LED on – waiting for external trigger LED off – receiving external trigger

Blink codes are used to signal warnings or error states:

Class S1 / Error code S2	Warning 1 blink	DCAM 2 blinks	MISC 3 blinks	FPGA 4 blinks	Stack 5 blinks
FPGA Boot error				1-5 blinks	
Stack setup					1 blink
Stack start					2 blinks
No FLASH object			1 blink		
No DCAM object		1 blink			
Register mapping		2 blinks			
VMode_ERROR_STATUS	1 blink				
FORMAT_7_ERROR_1	2 blinks				
FORMAT_7_ERROR_2	3 blinks				

The following sketch illustrates the series of blinks for a Format_7_error_1:

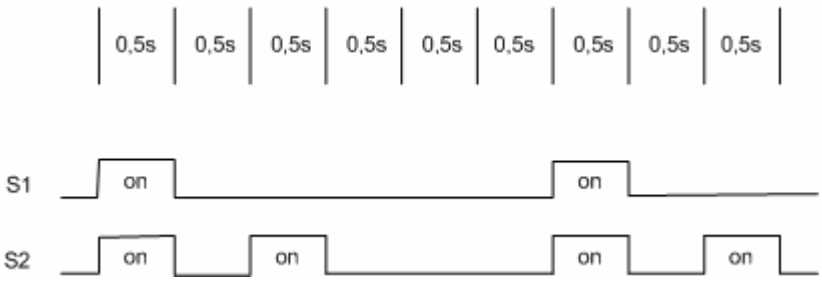


Figure 11 Warning and error states

You should wait for at least 2 full cycles because the display of blinking codes starts asynchronously – e.g. on the second blink from S2.

6.4 Operating the camera

Power for the camera is supplied either via the FireWire™ bus or via the HiRose plug. The input with the highest voltage provides power to the camera.

The input voltage must lie within the following range:

Vcc min.: + 8V
Vcc max.: +36V

ⓘ Input voltage of 12V is recommended to make most efficient use of the camera.

The camera does not supply voltage to the FireWire™ bus if it is being receiving power via the HiRose plug.

6.5 Control and video data signals

The camera has 3 inputs and 3 outputs. These can be configured via matching registers (see section 9.2.10 Input/Output pin control). The different modes are described below.

6.5.1 Inputs

All inputs have been implemented as shown on the diagram. IO_INP_CTRL1Polarity is controlled via the IO_INP_CTRL1..3 register (see section IO_INP_CTRL1)

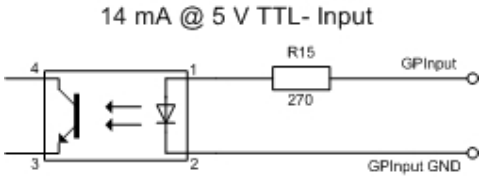


Figure 12 Diagram

Flux voltage from LED type 1.2V at 20 mA		Cycle delay of the optical coupler	
min. on-current:	5 mA	tpdHL:	38 µs
max. off-current:	1 mA	tpdLH:	780 ns
max. current:	50 mA		
max. input frequency:	2 kHz		
min. pulse width:	50 µs		

The inputs can be connected directly to +5V. If higher voltage is used a resistor will have to be switched in series.

+12 V 470 Ω
+24 V 1.2 kΩ

ⓘ Warning: Voltage above +45V may damage the optical coupler.

All input signals (Input 1...3) are inverted by the optical coupler.

All functions are listed in the following table

Function	Input 1	Input 2	Input 3
Trigger	X	x	x
Incremental decoder	INC0	INC1	INC Rst

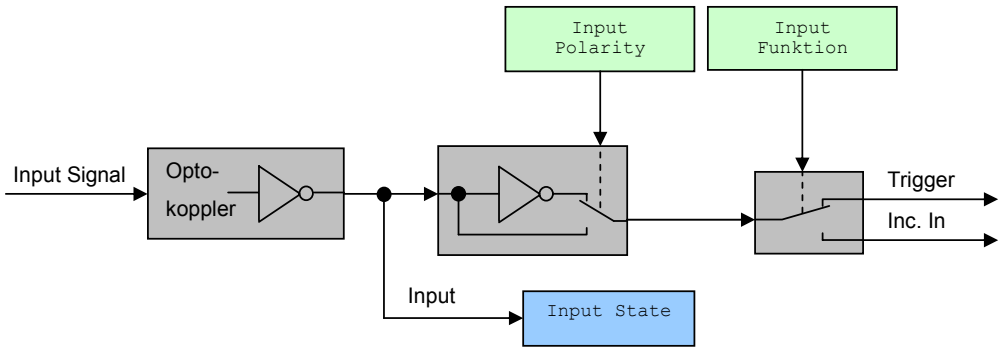


Figure 13 Block diagram of the inputs

Triggers

All inputs configured as triggers are linked by AND. If several inputs are being used as triggers, a high signal must be present on all inputs in order to generate a trigger signal. The polarity for each signal can be set separately via the inverting inputs.

The camera must be set to „external triggering“ to trigger image capture by the trigger signal.

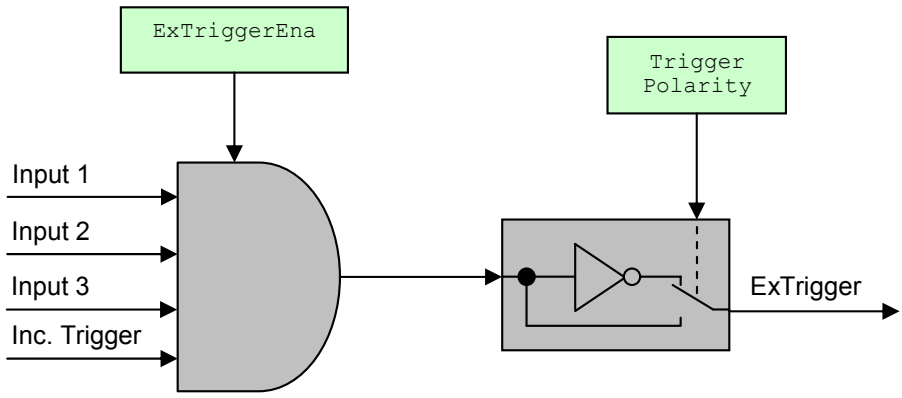


Figure 14 Trigger inputs

Incremental decoder

The decoder consists of a 12 bit counter. The counter uses the 3 hardware inputs.

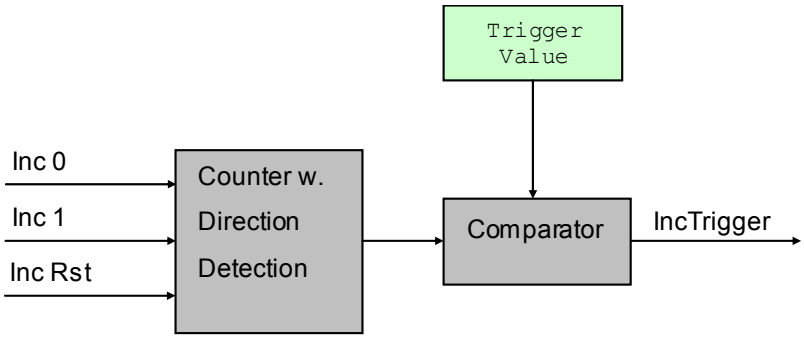


Figure 15 Incremental decoder

Input 1 is used for counting, input 2 for detecting the direction of rotation and input 3 for the reset signal. It counts upwards, if INC1 is "high" during a rising edge for INC0. It counts downwards, if INC1 is "low" during a rising edge for INC0. The counter can also be reset by command. The counter status can be read out.

When the counter reaches the comparator value, that can also be set by register, the output of the comparator is set, an internal trigger signal is generated and image capture activated. The camera must be configured for „external triggering“ for this to work.

The trigger signal is generated once the counter status reaches the comparator value.
A detailed register description can be found in Advanced features

6.5.2 Outputs

The camera has 3 inverted outputs with open collectors. These are shown with external wiring in the following diagram:

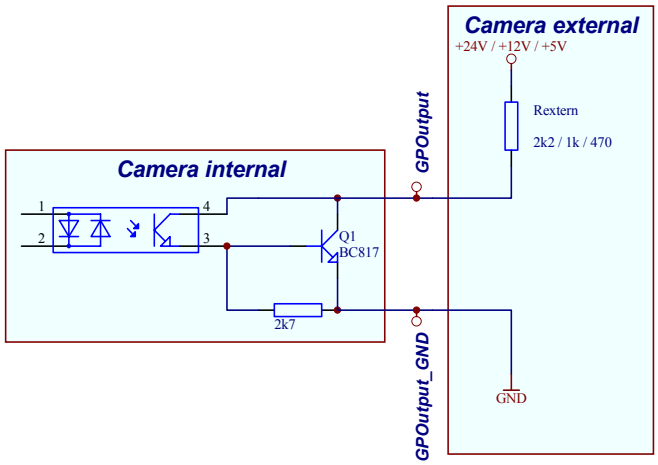


Figure 16 Camera outputs diagram

Max. collector voltage	500 mA
Max. collector emitter voltage	45 V

ⓘ Depending on the voltage applied a resistor may have to be switched in series (see diagram). Voltage above 45 V can damage the circuit.

Output features are configured by software.
Any signal can be placed on any output.

The main features of output signals are described below:

IntEna Signal
This signal displays the time the exposure was made. By using a register this output can be delayed by up to 1.05 seconds (see Enabling delayed integration).

Fval Signal
This feature signals readout from the sensor. This signal Fval follows IntEna.

Busy Signal
This indicator appears when the exposure is being made, the sensor is being read from or data transmission is active. The camera is busy.

Please refer to the following impulse diagram for information on how the individual signals are dependent on one another:

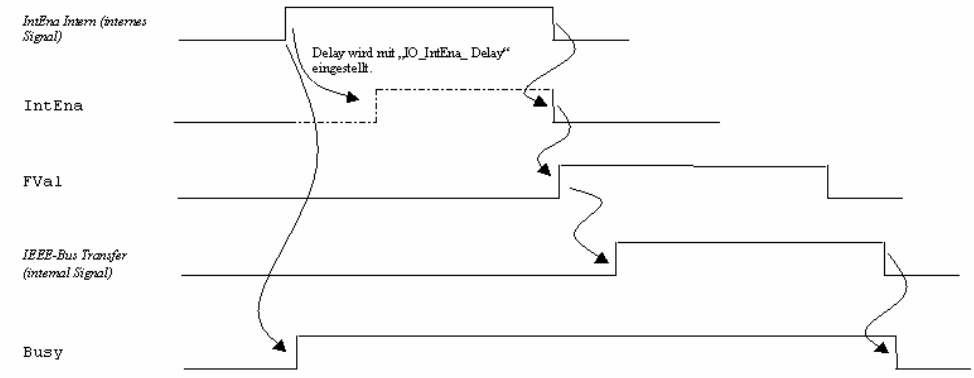


Figure 17 Impulse diagram

It is possible to use the IO_OUTP_CTRL1...3 register (see IO_OUTP_CTRL1) to assign a function to each output.

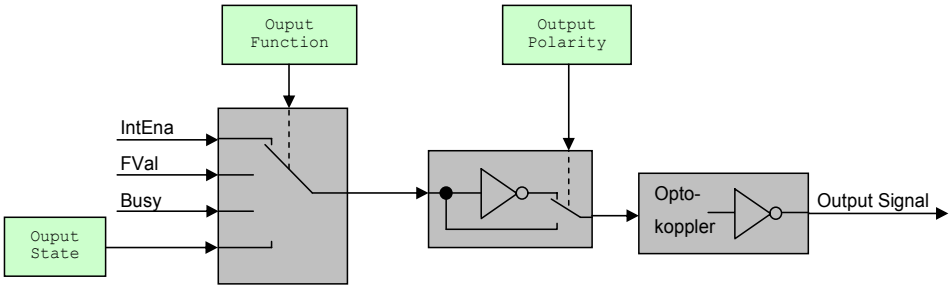
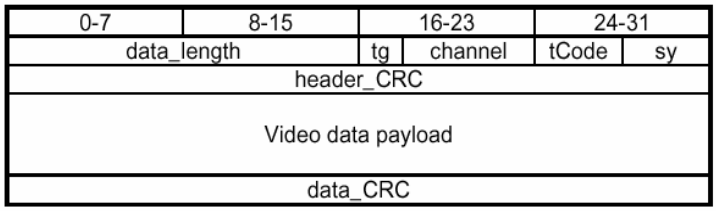


Figure 18 Camera outputs

6.5.3 Pixel Data

Pixel data is transmitted as isochronous data packets in accordance with the 1394 interface described in IIDC v. 1.3. The first packet of a frame is identified by the „1“ in the sync bit (sy) of the packet header.



Isochronous Data Block Packet Format

Figure 19 Isochronous data block packet format: Source: IIDC v. 1.3 specification

Video data for each pixel is output in 8 bit or 16 bit (10-bit data) format. Each pixel has a range of 256 or 1024 scales of gray. The digital value 0 is black and 255 or 1023 is white.

The following is a description of the video data format for the different modes. (Source: IIDC v. 1.3 specification)

<YUV (4: 2: 2) format >

U-(K+0)	Y-(K+0)	V-(K+0)	Y-(K+1)
U-(K+2)	Y-(K+2)	V-(K+2)	Y-(K+3)
U-(K+4)	Y-(K+4)	V-(K+4)	Y-(K+5)
U-(K+Pn-6)	Y-(K+Pn-6)	V-(K+Pn-6)	Y-(K+Pn-5)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	Y-(K+Pn-3)
U-(K+Pn-2)	Y-(K+Pn-2)	V-(K+Pn-2)	Y-(K+Pn-1)

<YUV (4: 1: 1) format >

U-(K+0)	Y-(K+0)	Y-(K+1)	V-(K+0)
Y-(K+2)	Y-(K+3)	U-(K+4)	Y-(K+4)
Y-(K+5)	V-(K+4)	Y-(K+6)	Y-(K+7)
U-(K+Pn-8)	Y-(K+Pn-8)	Y-(K+Pn-7)	V-(K+Pn-8)
Y-(K+Pn-6)	Y-(K+Pn-5)	U-(K+Pn-4)	Y-(K+Pn-4)
Y-(K+Pn-3)	V-(K+Pn-4)	Y-(K+Pn-2)	Y-(K+Pn-1)

Figure 20 YUV 4:2:2 and YUV 4:1:1 format: Source: IIDC v. 1.3 specification

<Y (Mono) format >

Y-(K+0)	Y-(K+1)	Y-(K+2)	Y-(K+3)
Y-(K+4)	Y-(K+5)	Y-(K+6)	Y-(K+7)
Y-(K+Pn-8)	Y-(K+Pn-7)	Y-(K+Pn-6)	Y-(K+Pn-5)
Y-(K+Pn-4)	Y-(K+Pn-3)	Y-(K+Pn-2)	Y-(K+Pn-1)

< Y (Mono16) format >

High byte	Low byte

Y-(K+0)	Y-(K+1)
Y-(K+2)	Y-(K+3)
Y-(K+Pn-4)	Y-(K+Pn-3)
Y-(K+Pn-2)	Y-(K+Pn-1)

Figure 21 Y8 and Y16 format: Source: IIDC v. 1.3 specification

<Y, R, G, B>

Each component has 8bit data. The data type is "Unsigned Char".

	Signal level (Decimal)	Data (Hexadecimal)
Highest	255	0xFF
	254	0xFE
	:	:
	1	0x01
Lowest	0	0x00

<U, V>

Each component has 8bit data. The data type is "Straight Binary".

	Signal level (Decimal)	Data (Hexadecimal)
Highest (+)	127	0xFF
	126	0xFE
	:	:
	1	0x81
Lowest	0	0x80
	-1	0x7F
	:	:
	-127	0x01
Highest (-)	-128	0x00

< Y(Mono16) >

Y component has 16bit data. The data type is "Unsigned Short (big-endian)".

Y	Signal level (Decimal)	Data (Hexadecimal)
Highest	65535	0xFFFF
	65534	0xFFFE
	:	:
	1	0x0001
Lowest	0	0x0000

Figure 22 Data structure: Source: IIDC v. 1.3 specification

6.6 Time response

The following sections describe time response of the camera using a single frame (OneShot) command. As set out in the IIDC specification, this is a software command that causes the camera to record and transmit a single frame.

6.6.1 OneShot command on the bus to start of exposure

The following values apply only under the condition that the camera is idle and ready for use. Full resolution must also be set.

OneShot->Microcontroller-Sync: < 600 µs (processing time in the microcontroller)

µC-Sync/ExSync->Integration-Start 8µs

Microcontroller-Sync is an internal signal. It is used by the microcontroller to initiate a trigger. This can either be a direct trigger or a release for ExSync if the camera is triggered externally.

6.6.2 End of exposure to first packet on the bus

After the exposure the CCD is read out and some data is written into the FRAME_BUFFER before being transmitted to the bus.

The time from the end of exposure to the start of transport on the bus is:

488µs ± 62.5µs

This time jitters with the cycle time of the bus (125µs).

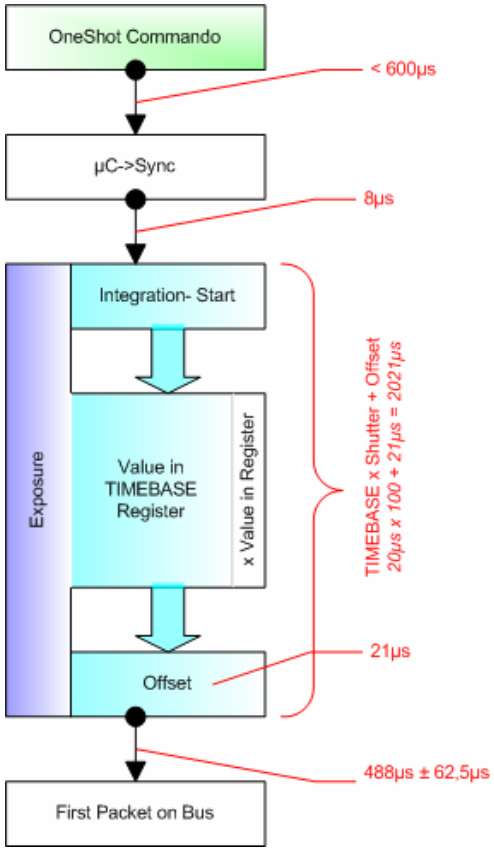


Figure 23 chronological sequence after end of exposure

6.6.3 Exposure time

The exposure time is based on the following formula:

Register value x Timebase + Offset

The register value is the value set in the corresponding IIDC register (SHUTTER [81Ch]). This number lies in the range between 1 and 4095.

The Shutter register value is multiplied by the Time base register value (see TIMEBASE). The default value here is set to 20µs.

A camera-specific offset of 21 µs is also added to this value

Example

Register value: 100
Timebase: 20 µs

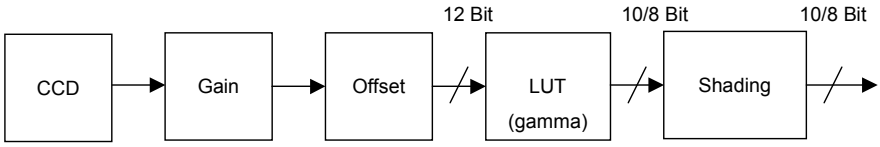
100 x 20 µs + 21 µs = 2021 µs exposure time.
The minimum adjustable exposure time set by register is 10µs. => the real minimum exposure time of an F-145b is then 10µs + 21µs = 31µs.

7 Block diagrams of the camera

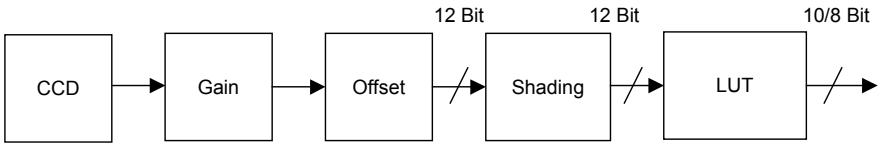
7.1 Description of the data path

In the following diagrams you can see the data flow and the bit resolution of image data after being read from the CCD chip in the camera. The individual steps are described in more detail in the following paragraphs.

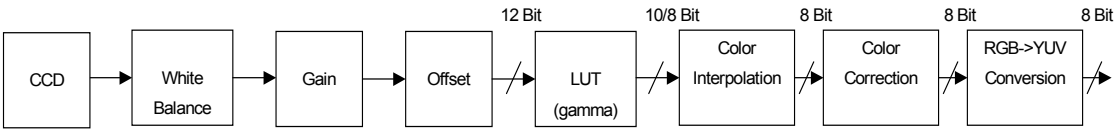
F-145B up to FW 0.83



F-145B from FW 0.84



F-145C



7.2 White balance

The color cameras have both manual and automatic white balance, that can be set via the analog red and blue gain in the 0...+10 dB range. White balance is used so that non colored image parts are displayed non colored.

These settings are made in register 80C of IIDC v. 1.3. The values in the *V_Value/R_Value* field produce changes in the gain from green to red and in the *U_Value/B_Value* field from green to blue.

Values in the 0...53 range may be entered.

7.2.1 Automatic white balance

Automatic white balance is activated by setting the "One Push" bit in the WHITE_BALANCE register (see WHITE-BALANCE). The camera independently inputs frames and calculates the U/B and V/R correction values on the basis of 16x16 pixels from the center of the currently set frame.

For white balance incoming frames are input based on the current settings of all registers (GAIN, OFFSET, SHUTTER, etc.).

The following ancillary conditions should be observed for successful white balance:

- All pixels in the 16x16 calculation window must have a gray value <255 and the object in the calculation window must be monochrome.

- Automatic white balance can be started both during active image capture and also when the camera is in idle state.

If the image capture is active (e.g. "IsoEnable" set in register 614h), the frames used by the camera for white balance are also output on the 1394 bus. Any previously active image capture is started again after the completion of white balance.

Automatic white balance can also be started by using an external trigger. However, if there is a pause of >10 seconds between capturing individual frames the process is aborted.

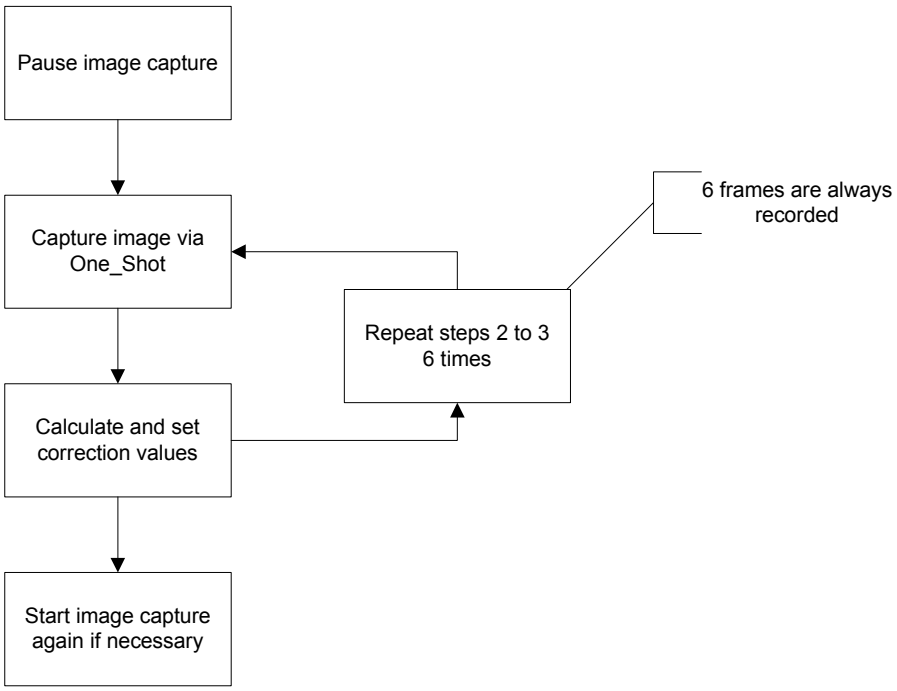


Figure 24 Automatic white balance sequence

Finally, the calculated correction values can be read from the WHITE_BALANCE register.

ⓘ Automatic white balance does not work in Mono16 (10 Bit) mode.

7.3 Manually setting gain

The following ranges can be used when manually setting the gain for the analog video signal:

F-145B	0...+29 dB
F-145C	0...+24.4 dB

The increment length is ~0.0354 dB/step.

The values to be entered lie within the following ranges:

F-145B	0 ... 820
F-145C	0 ... 690

ⓘ Setting the gain can be done independently from setting the offset (black value).

ⓘ Higher gain also produces greater image distortion. This reduces image quality. This is why you should first try to increase the brightness using the aperture of the camera optics and shutter settings.

7.4 Setting the offsets (black value)

It is possible to set the black value in the camera within the following ranges:

0...+16 gray values (8 bit)
0...+64 gray values (10 bit)

Increments are in ¼ LSB (8 bit) or ½ LSB (10 bit).

The formula for gain and offset setting is:

Y`= GxY+0

7.5 Lookup tables (LUT)

The camera provides support for up to 63 user-defined LUTs. An additional lookup table is used for implementing gamma correction. The lookup tables convert the 12 bits from the digitizer to 10 bits. Starting with FW 0.84 the LUT output can also be 12 bit on the F-145B.

The use of LUTs allows you to store any function in the form Output = F(Input) in the RAM of the camera and to use it on the individual pixels of the frame at run-time.

These make it possible to carry out complex calculations at a suitable point in time and to use the results while operating the camera in real time. The values of functions are calculated within a specific range and the input value is used as an index in the table.

The AVT Dolphin can temporarily store up to 64 LUTs in the camera. One example of such an LUT is the gamma LUT.

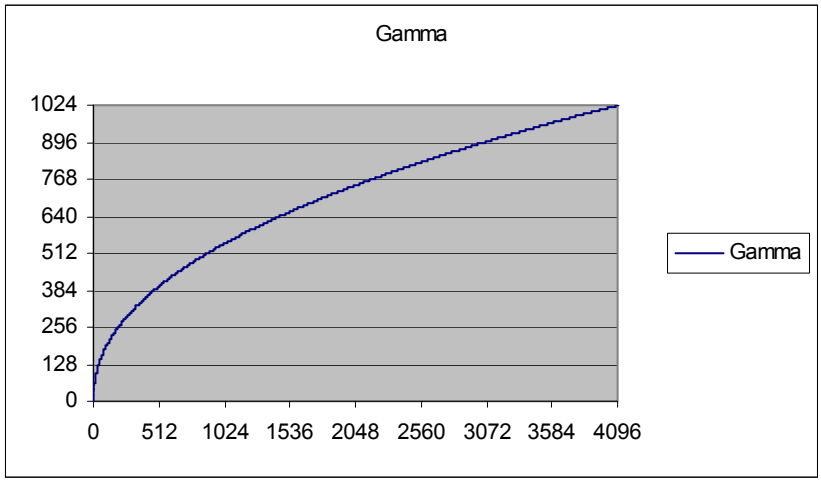


Figure 25 Gamma LUT

ⓘ The input value is a 12-bit value from the digitizer. The output value is a value of 8, 10 or 12 bits, depending on the video format and mode.

ⓘ Because gamma correction is also internally implemented via a lookup table and only one lookup table can be active at the same time, it is not possible to use a different LUT when gamma correction is switched on.

Loading a LUT into the camera

Loading is done through the GPDATA_BUFFER data exchange buffer. Because the buffer can hold only a maximum of 2 kB and is smaller than a complete LUT at 4096 x 16 bit (8 kB), writing must take place in several steps:

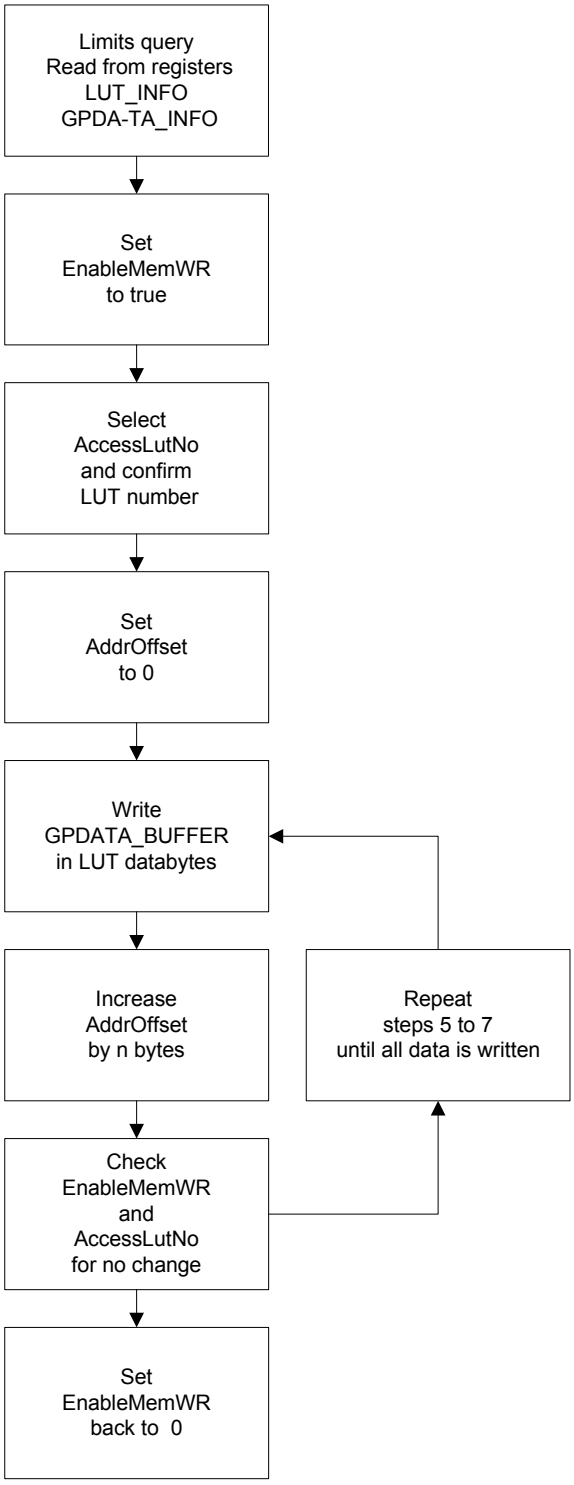


Figure 26 Loading a LUT

7.6 Shading correction

Shading correction is used to compensate for inhomongeneities caused by lighting or optical characteristics within specified ranges. To correct a frame, a multiplier from 1...2 is calculated for each pixel in 1/256 steps – this allows for shading to be compensated by up to 50%.

Besides offline generating shading data and download it to the camera, the camera allows correction data to be generated automatically in the camera itself.

7.6.1 Automatic generation of correction data

Requirements
Shading correction compensates for inhomongeneities by giving all pixels the same gray value as the brightest pixel. This means that only the background may be visible and the brightest pixel has a gray value of less than 255 when automatic generation of shading data is started.

Algorithm
After the start of automatic generation the camera pulls in the number of frames set in the GRAB_COUNT register. An arithmetic mean value is calculated from them (to reduce noise).

After this, a search is made for the brightest pixel in the mean value frame. A multiplier is calculated for each pixel to be multiplied by, giving it the gray value of the brightest pixel.

All of these multipliers are saved in a "Shading Reference Image". The time required for this process depends on the number of frames to be calculated.
Correction alone can compensate for shading by up to 50% and counts on 10 or 12 bit pixel data (beginning with FW 0.84) to avoid the generation of missing codes.

The calculation of shading data is always carried out at the current resolution set. If the Area of Interest is bigger than the window in which correction data was being calculated, none of the pixels lying outside are corrected.

For Format_7 it is advisable to generate the shading image in the largest displayable frame format. This ensures that even any smaller Areas of Interest (AOIs) are completely shading corrected. The automatic generation of shading data can also be started when image capture is running. The camera then pauses the running image capture for the time needed for generation and resumes it after generation is completed.

Automatic generation of a shading image
As previously mentioned, shading images can also be generated by the camera. Before using this feature you should make sure that frame size is set to maximum and brightness is set so that the frame is not overmodulated. It may be necessary to use a neutral white reference, e.g. a piece of paper, instead of the real image.

How to proceed:

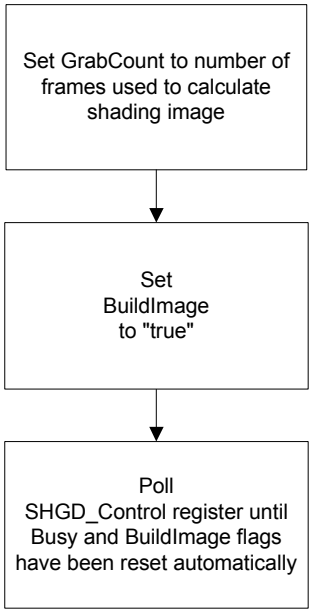


Figure 27 automatic generation of a shading image

ⓘ The maximum value of GRAB_COUNT depends on the type of camera and the number of existing frame buffers. GRAB_COUNT is also automatically corrected to the power of two.

ⓘ The SHDG_CTRL register should not be queried at very short intervals, because each query delays the generation of the shading image. A good interval time is 500 ms.

The following pictures clarify the process of automatic generation of correction data. The characteristic curves were created using MVTEC's "ActivVision Tools".

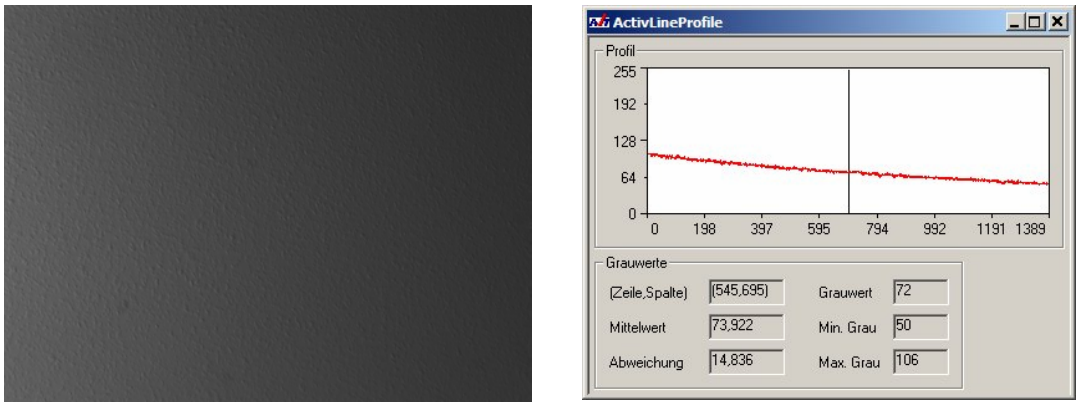
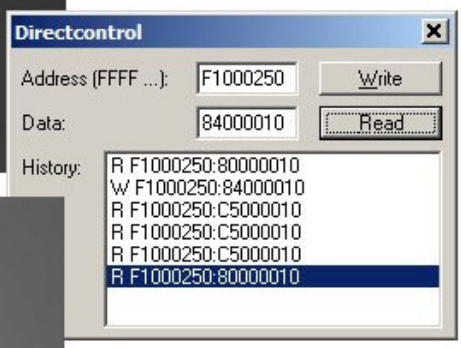


Figure 28 Source image with non-uniform illumination

On the left you see the source image with non-uniform illumination. The line view in the picture on the right clearly shows the brightness level falling off to the right.

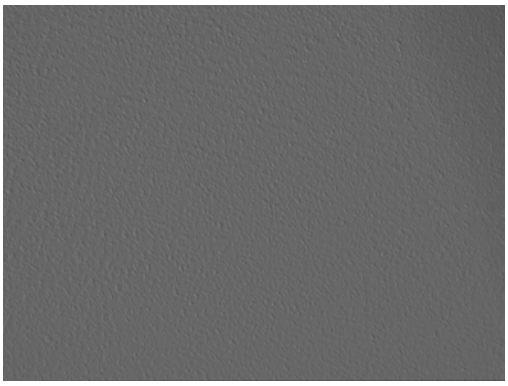
The correction sequence controlled via "Directcontrol" uses the average of 16 frames (10H) to calculate the correction frame. By unfocussing the lens high-frequency image data is removed from the source image, keeping it from being contained in the shading image.

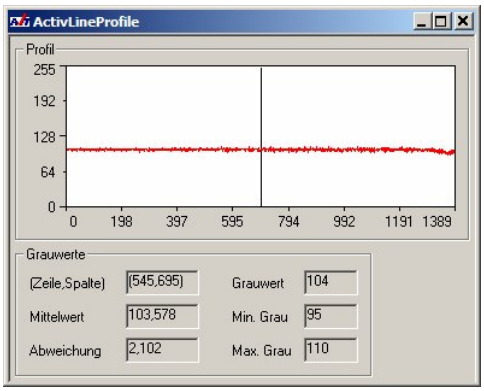
Source image set unfocused



Shading corrected output image
(unfocused lens)

After the lens has been focused again you see the previous image, but now with a considerably more uniform gradient. This is also made apparent in the line view.





Loading a shading image into the camera

GPDATA_BUFFER is used to load a shading image into the camera. Because the size of a shading image is larger than GPDATA_BUFFER input must be handled in several steps:

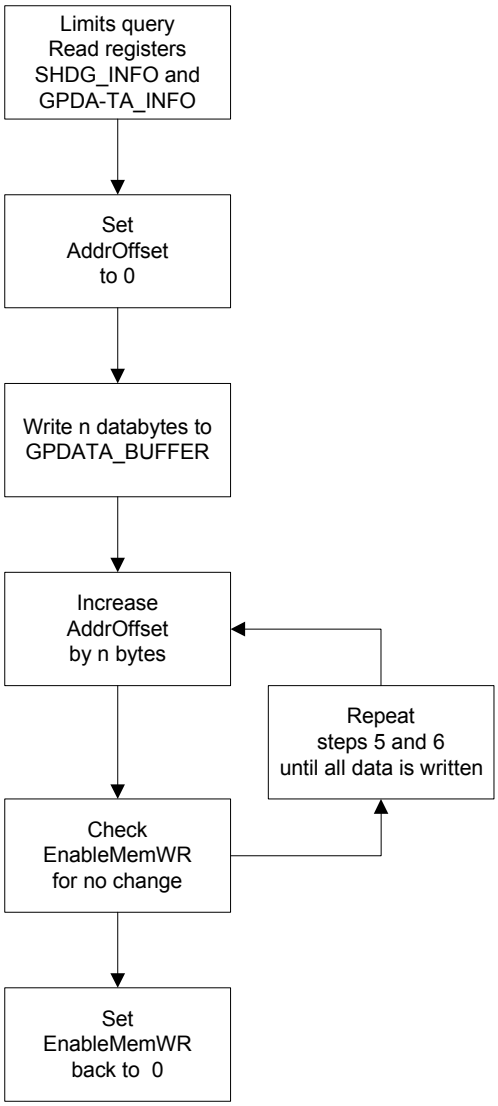


Figure 29 Loading a shading image

7.7 Color interpolation and correction

In the sensors used color information is captured via the primary color filters placed over the individual pixels in a "BAYER mosaic" layout. Simple Bayer -> RGB color interpolation already takes place in the Dolphin F-145C color version. When converting to the YUV format color correction is done at the same time.

Interpolation (BAYER demosaicing)

In interpolation a red, green or blue value is determined for each pixel. Only two lines are used for this simple interpolation:

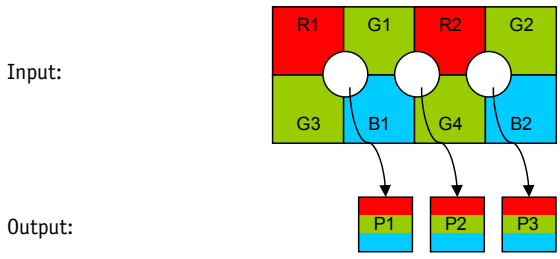


Figure 30 Interpolation

$$P1_{red} = R1 \qquad P2_{red} = R2 \qquad P3_{red} = R2$$
$$P1_{green} = \frac{G1+G3}{2} \qquad P2_{green} = \frac{G1+G4}{2} \qquad P3_{green} = \frac{G2+G4}{2}$$
$$P1_{blue} = B1 \qquad P2_{blue} = B1 \qquad P3_{blue} = B2$$

Color cameras begin outputting the image in line two and finish in line Y (maximum image height minus two). This is a side-effect of BAYER demosaicing. The adjustable maximum image height is also two lines less than in the b/w variant.

ⓘ Please note that on the color camera a black border one pixel wide forms on the left and right image borders also as a consequence of BAYER demosaicing, because the image width displayed on the color camera is not scaled down.

Color correction
Color correction is calculated along with YUV conversion and mapped via a matrix like this.

$$red^* = Crr \cdot red + Cgr \cdot green + Cbr \cdot blue$$
$$green^* = Crg \cdot red + Cgg \cdot green + Cbg \cdot blue$$
$$blue^* = Crb \cdot red + Cgb \cdot green + Cbb \cdot blue$$

On the color camera color correction is also deactivated in Mono8 or Mono16 mode (raw image transport).

7.7.1 RGB → YUV conversion

The conversion from RGB to YUV is done using the following formula:

$$Y = 0.3 \cdot R + 0.59 \cdot G + 0.11 \cdot B$$
$$U = -0.169 \cdot R - 0.33 \cdot G + 0.498 \cdot B + 128$$
$$V = 0.498 \cdot R - 0.420 \cdot G - 0.082 \cdot B + 128$$

7.8 Controlling image capture

The camera supports the SHUTTER_MODES specified in IIDC v. 1.3. Each mode can be combined with an external trigger. In this case individual images are recorded when an external trigger impulse is present.

7.8.1 OneShot

The camera can record an image by setting “OneShot” in the 61Ch register. This bit is automatically cleared after the image is captured. If the camera is placed in *Iso_Enable* mode (see ISO_Enable / Free-Run), this flag is ignored.
If *OneShot mode* is combined with the external trigger, the “OneShot” command is used to arm it. If the trigger impulse is absent being armed, OneShot can be cancelled by clearing the bit.

7.8.2 Multi-Shot

Setting “MultiShot” and entering a quantity of images in *Count_Number* in the 61Ch register enables the camera to record a specified number of images.

The number is indicated in bits 16 to 31. If the camera is put into *Iso_Enable* mode (ISO_Enable / Free-Run), this flag is ignored and is deleted automatically once all of the images have been recorded.

If *MultiShot* mode is activated and the images are not yet finished being captured it can be quit by resetting the flag. The same can be achieved by setting the number of images to “0”.

7.8.3 ISO_Enable / Free-Run

Setting the “0” bit in the 614h register (ISO_ENA) puts the camera into *ISO_Enable mode* or *Continuous_Shot*. The camera captures a series of images. This operation can be quit by deleting the “0” bit.

7.8.4 Asynchronous broadcast

The camera accepts asynchronous broadcasts. This involves asynchronous write or read requests that use node number 63 as the target node.

This makes it possible for all cameras on a bus to be triggered by software simultaneously - e.g. by broadcasting a “One_Shot”. All cameras receive the “One_Shot” command in the same cycle.

7.8.5 Jitter at start of exposure

Uncertainty over the actual start of exposure depends on the state of the camera. A difference is made:

FVal is active	→	the sensor is reading out
FVal is inactive	→	the sensor is ready, the camera is idle

If the sensor is ready a fixed time of 100 ns passes before the exposure begins. If the sensor is reading out, the time until the exposure starts varies by the length of one line.

Thus, a maximum delay of 63.7 µs can occur.

FVal state	F-145B	F-145C
Low	100 ns	100 ns
High	63.7 µs	63.7 µs

ⓘ Jitter at the beginning of exposure has no effect on the length of exposure time, i.e. it is always constant.

7.9 Sequence mode

The camera enables certain image settings to be set differently for a succession of images.

For a sequence of images with different lighting colors each image can be recorded with a different gain to obtain the same brightness effect. The image area of a sequence of images can automatically be separated into several smaller ones by varying the AOI.

A parameter set is stored in the camera for each image to be recorded. This sequence of parameter sets is simply called a sequence.

The following registers can be used to effect the individual steps of the sequence.

All modes	Cur_V_Mode, Cur_V_Format, ISO_Channel, ISO_Speed, Brightness, White_Balance (color cameras only), Shutter, Gain, Lookup- Table, TestImage
Fixed modes only	Cur_V_Frm_Rate
Format_7 only	Image_Position, Image_Size, Color_Coding_ID, Byte_Per_Packet, Binning

7.9.1 How is sequence mode implemented?

There is a FIFO (first in first out) memory for each of the IIDC v. 1.3 registers listed above. The depth of each FIFO is determined by the maximum number of images contained in the sequence.

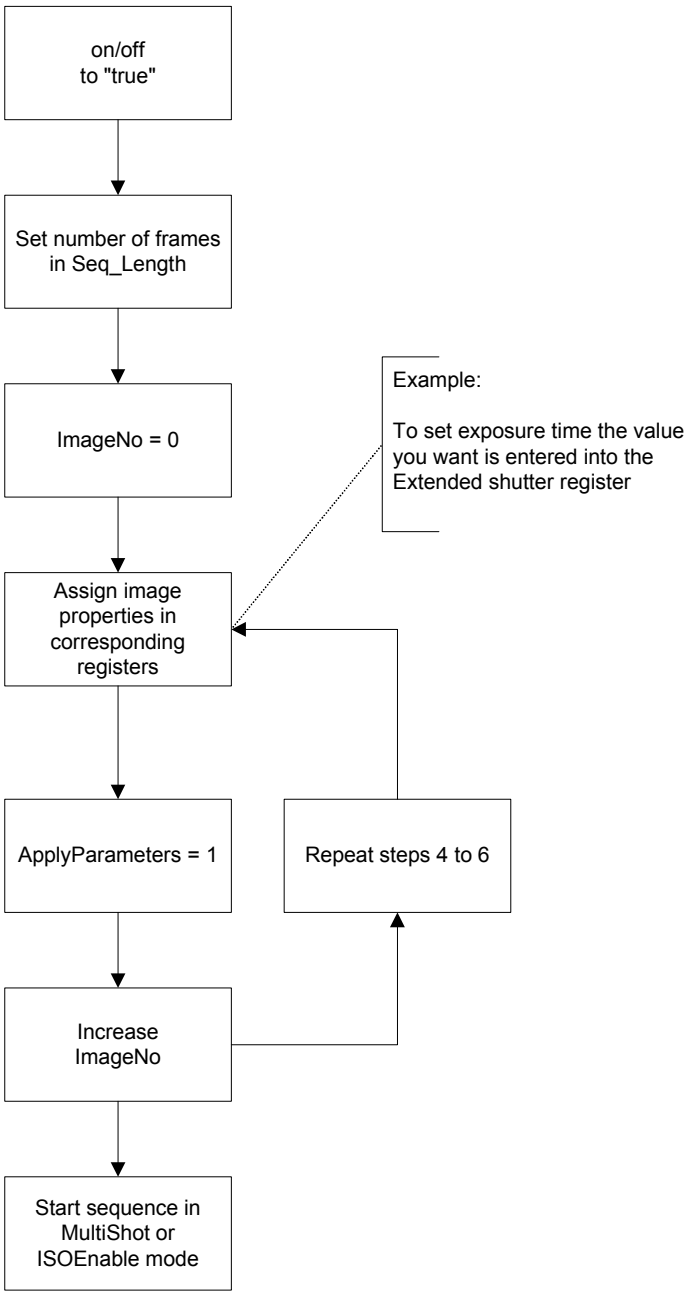


Figure 31 Sequence mode

During this process the camera gets the required parameters image by image from the corresponding FIFOs (e.g. information for exposure time)

ⓘ The appearance of the images is based on the data from the FIFOs. This also applies when less sensible, invalid or no data at all are stored in memory.

ⓘ If more images are recorded than data sets are stored in the sequence, the last parameters are applied to all additional images

ⓘ If *sequence* mode is quit, the camera can use the FIFO for other tasks. For this reason, a sequence must be loaded back into the camera after *sequence* mode has been quit.

7.9.2 Reading in the sequence

Reading in sequence parameters for the image takes place in parallel to the process of generating and transporting the image.

Figure 32 Reading in the sequence

What to pay attention to when working with a sequence:

ⓘ If more images are recorded than defined in *SeqLength* the settings for the last image remain in effect.

ⓘ To repeat the sequence, stop the camera and send the “MultiShot” or “IsoEnable” command again. Each of these two commands resets the sequence.

ⓘ Using *SingleShot* mode in combination with a sequence does not make sense, because *SingleShot* mode restarts the sequence every time.

ⓘ The sequence may not be active when setting the *AutoRewind* flag. For this reason it is important to set the flag before the “MultiShot” or “ISO_Enable” commands.

ⓘ If the sequence is used with the *deferred transport* feature the number of images entered in *Seq_Length* may not be exceeded. (see Deferred image transport)

7.9.3 Changing the parameters within a sequence

It is not necessary to make settings for the entire sequence to change the parameters within a sequence . The image can simply be selected via the *ImageNo* field and then to change the corresponding IIDC v. 1.3 register.

What to pay attention to when changing the parameters:

ⓘ If the *ApplyParameters* flag is used when setting the parameters all not-configured values are set to default values. Because changing a sequence normally affects only the value of a specific register and all other registers should not be changed, the *ApplyParameters* flag may not be used here.

ⓘ The values stored for individual images can no longer be read.

ⓘ If the camera is switched into *sequence mode* , the changes to the IIDC v. 1.3 register for the image specified in *ImageNo* take effect immediately.

7.10 Deferred image transport

An image is normally captured and transported in consecutive steps. The image is taken, read out from the sensor, digitized and sent over the 1394 bus.

This order of events can be paused or delayed by using the *deferred image transport* feature. 2 modes are available. Both can also be used at the same time – but only in Format_7.

7.10.1 HoldImg mode

By setting the *HoldImg* flag transport of the image over the 1394 bus is stopped completely. All captured images are stored in the internal ImageFIFO. The camera reports the maximum possible number of images in the FiFoSize variables.

- Pay attention to the maximum number of images that can be stored in FIFO. If you capture more images than the number in FiFoSize, the oldest ones are overwritten.
- The extra *SendImage* flag is set to “true” to import the images from the camera. The camera sends the number of images that are entered in the *NumOfImages* parameter.
- If *NumOfImages* is “0” all images stored in FIFO are sent.
- If *NumOfImages* is not “0”, the corresponding number of images are sent.
- If the *HoldImg* field is set to “false”, all images in *ImageFIFO* are deleted. No images are sent.

7.10.2 FastCapture

This mode can be activated in Format_7 only.

When *FastCapture* is set to “false”, the maximum frame rate is associated with the packet size set in the BYTE_PER_PACKET register. The lower this value, the lower the attainable frame rate.

By setting *FastCapture* to “true“ all images are recorded at the highest possible frame rate, i.e. the setting above does not effect the frame rate.

8 Video formats, video modes and IEEE 1394 bandwidth

Video modes – F-145B

For-mat	Mode	Resolution	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps[1]
0	0	160 x 120 YUV444						
	1	320 x 240 YUV422						
	2	640 x 480 YUV411						
	3	640 x 480 YUV422						
	4	640 x 480 RGB						
	5	640 x 480 MONO 8			x	x	x	
	6	640 x 480 MONO 16			x	x	x	
1	0	800 x 600 YUV422						
	1	800 x 600 RGB						
	2	800 x 600 MONO8			x	x		
	3	1024 x 768 YUV422						-
	4	1024 x 768 RGB						-
	5	1024 x 768 MONO 8			x	x	x	-
	6	800 x 600 MONO 16			x	x	x	
	7	1024 x 768 MONO 16			x	x	x	-
2	0	1280 x 960 YUV422						
	1	1280 x 960 RGB						
	2	1280 x 960 MONO 8			x	x	x	x
	3	1600 x 1200 YUV422						
	4	1600 x 1200 RGB						
	5	1600 x 1200 MONO 8						
	6	1280 x 960 MONO 16				x	x	x
	7	1600 x 1200 MONO 16						

7	0	1392x 1040 MONO8/16	
	1	696 x 1040 MONO8/16	Horizontal binning
	2	1392 x 520 MONO8/16	Vertical binning
	3	696 x 520 MONO8/16	Vertical + horizontal binning (2x2)

[1)] Conditional on the maximum number of 4095 packets/frame, not possible in all formats.

Video modes – F-145C

For-mat	Mode	Resolution	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
0	0	160 x 120 YUV444						
	1	320 x 240 YUV422			x	x	x	
	2	640 x 480 YUV411			x	x	x	
	3	640 x 480 YUV422			x	x	x	
	4	640 x 480 RGB						
	5	640 x 480 MONO 8			x	x	x	
	6	640 x 480 MONO 16			x	x	x	
1	0	800 x 600 YUV422			x	x	x	
	1	800 x 600 RGB						
	2	800 x 600 MONO8			x	x		
	3	1024 x 768 YUV422			x	x	x	-
	4	1024 x 768 RGB						-
	5	1024 x 768 MONO 8			x	x	x	-
	6	800 x 600 MONO 16			x	x	x	
	7	1024 x 768 MONO 16			x	x	x	-
2	0	1280 x 960 YUV422				x	x	x
	1	1280 x 960 RGB						
	2	1280 x 960 MONO 8			x	x	x	x
	3	1600 x 1200 YUV422						
	4	1600 x 1200 RGB						
	5	1600 x 1200 MONO						
	6	1280 x 960 MONO 16				x	x	x
	7	1600 x 1200 MONO 16						
7	0	1392x 1038 YUV411/422						
	1	1392 x 1040 MONO8/16						

Due to color interpolation the maximum height is 1038 pixels and the first and last pixel columns contain no image information.

8.1 Area of interest (AOI)

The image sensor on the camera has a defined resolution. This indicates the maximum number of lines and pixels per line that the recorded image may have.

However, often only a certain section of the entire image is of interest. The amount of data to be transferred can be decreased by limiting the image to a section when reading it out from the camera. At a lower vertical resolution the sensor can be read out faster and thus the frame rate is increased.

ⓘ The setting of AOIs is supported only in video Format_7.

While the size of the image read out for most other video formats and modes is fixed by the IIDC specification, thereby determining the highest possible frame rate, in Format_7 the user can set the “upper left corner” and “width and height” of the section (Area of Interest) he is interested in to determine the size and thus the highest possible frame rate.

Setting the AOI is done in the IMAGE_POSITION and IMAGE_SIZE registers.
Attention should be paid to the increments entered in the UNIT_SIZE_INQ and UNIT_POSITION_INQ registers when configuring IMAGE_POSITION and IMAGE_SIZE.

IMAGE_POSITION and IMAGE_SIZE contain in the respective bits values for the column and line of the upper left corner and values for the width and height.

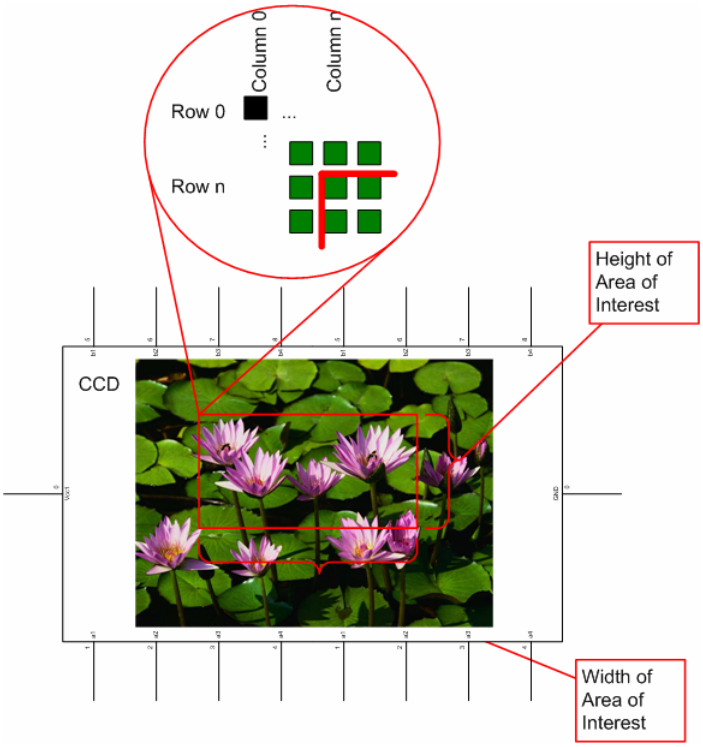


Figure 33 Area of Interest

ⓘ The left position + width and the upper position + height may not exceed the maximum resolution of the sensor.

ⓘ The coordinates for width and height must be divisible by 8.

In addition to the Area of Interest still other parameters have an effect on the maximum frame rate

- the time for reading the image from the sensor and transporting it in the FRAME_BUFFER
- the time for transferring the image over the FireWire™ bus
- the length of the exposure time

8.2 Binning

Binning is the process of combining neighboring pixels while being read out from the CCD chip. This is done primarily for 3 reasons:

- A reduction in the number of pixels and thus the amount of data when retaining the original image area angle,
- an increase in the frame rate,
- an improvement in the separation of signal to noise.

Signal to noise ratio (SNR) and signal to noise separation specify the quality of a signal with regard to its reproduction of intensities. The value signifies how high the ratio of noise is in regard to the maximum wanted signal intensity expected.

The higher this value, the better the signal quality. The unit of measurement used is generally known as the decibel (dB), a logarithmic power level. 6 dB is the signal level at approximately a factor of 2.

However, the advantages of increasing signal quality are accompanied by a reduction in resolution.

Binning is possible only in video Format_7. The type of binning used depends on the video mode. In general a difference is made between two types of binning, that can also be combined:

8.2.1 Vertical binning

Vertical binning increases the light sensitivity of the camera by a factor of two by adding together the values of two adjoining vertical pixels output as a single pixel. At the same time this normally improves signal to noise separation by about 2 dB.

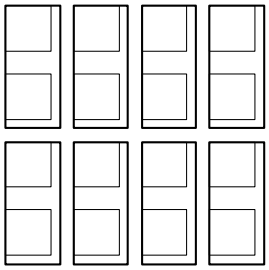


Figure 34 Vertical binning

This reduces vertical resolution to 520 lines.

If vertical binning is activated the image may appear to be over-exposed and must be corrected.

The color sensor of the F-145C does NOT support binning mode.

8.2.2 Horizontal binning

In horizontal binning adjacent horizontal pixels in a line are combined in pairs.

This means that in horizontal binning the light sensitivity of the camera is also increased by a factor of two (6 dB). Signal to noise separation improves by approx. 3 dB. Horizontal resolution is lowered to 696 pixels.

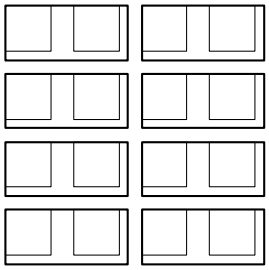


Figure 35 Horizontal binning

8.2.3 Full binning

If horizontal and vertical binning are combined, every 4 pixels are consolidated into a single pixel. At first two horizontal pixels are put together and then combined vertically.

This increases light sensitivity by a total of a factor of 4 and at the same time signal to noise separation is improved by about 6 dB. Resolution is reduced to 696 x 520 pixels.

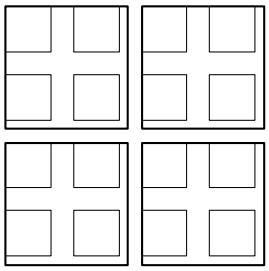


Figure 36 Full binning

8.3 Frame rates

An IEEE-1394 camera requires bandwidth to transport images.

The IEEE-1394a bus has very large bandwidth of at least 32 MB/s for transferring (isochronously) image data.

Depending on the video format settings and the configured frame rate the camera requires a certain percentage of maximum available bandwidth.

The following tables indicate how much data in various formats and modes can be sent within one cycle (125µs) at 400 Mb/s of bandwidth.

They enable you to calculate the required bandwidth and to ascertain the number of cameras that can be operated independently on a bus and in what mode.

Format	Mode	Resolution	60 fps	30 fps	15 fps	7.5 fps	3.75 fps
0	0	160 x 120 YUV (4:4:4) 24 bit/pixel		1/2H 80p 60q	1/4H 40p 30q	1/8H 20p 15q	
	1	320 x 240 YUV (4:2:2) 16 bit/pixel		1H 320p 160q	1/2H 160p 80q	1/4H 80p 40q	1/8H 40p 20q
	2	640 x 480 YUV (4:1:1) 12 bit/pixel		2) 2H 1280p 480q	1H 640p 240q	1/2H 320p 120q	1/4H 160p 60q
	3	640 x 480 YUV (4:2:2) 16 bit/pixel		4) 2H 1280p 640q	2) 1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q
	4	640 x 480 RGB 24 bit/pixel		4) 2H 1280p 960q	2) 1H 640p 480q	1/2H 320p 240q	1/4H 160p 120q
	5	640 x 480 (MONO) 8 bit/pixel	4) 4H 2560p 640q	2) 2H 1280p 320q	1H 640p 160q	1/2H 320p 80q	1/4H 160p 40q
	6	640 x 480 Y (MONO 16) 16 bit/Pixel		4) 2H 1280p 640q	2) 1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q
	7	640 x 480 Y (MONO 16) Reserved					

For-mat	Mode	Resolution	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
1	0	800 x 600 YUV (4:2:2) 16 bit/pixel		4)5/2H 2000p 1000q	2)5/4H 1000p 500q	5/8H 500p 250q	6/16H 250p 125q	
	1	800 x 600 RGB 24 bit/Pixel			4)5/4H 1000p 750q	2)5/8H 500p 375q		
	2	800 x 600 Y (MONO) 8 bit/pixel	4) 5H 4000p 1000q	2)5/2H 2000p 500q	5/4H 1000p 250q	5/8H 500p 125q		
	3	1024 x 768 YUV (4:2:2) 16 bit/pixel			4)3/2H 1536p 768q	2)3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q
	4	1024 x 768 RGB 24 bit/pixel				4)3/4H 768p 576q	2)3/8H 384p 288q	3/16H 192p 144q
	5	1024 x 768 Y (MONO) 8 bit/pixel)		4)3H 3072p 768q	2)3/2H 1536p 384q	3/4H 768p 192q	3/8H 384p 96q	3/16H 192p 48q
	6	800 x 600 (MONO 16) 16 bit/pixel)		4)5/2H 2000p 1000q	2)5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
	7	1024 x 768 Y(MONO 16) 16 bit/pixel			4)3/2H 1536p 768q	2)3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q

For-mat	Mode	Resolution	60 fps	30 fps	15 fps	7.5 fps	3.75 fps	1.875 fps
2	0	1280 x 960 YUV (4:2:2) 16 bit/pixel				4)1H 1280p 640q	2)1/2H 640p 320q	1/4H 320p 160q
	1	1280 x 960 RGB 24 bit/pixel				4)1H 1280p 960q	2)1/2H 640p 480q	1/4H 320p 240q
	2	1280 x 960 Y (MONO) 8 bit/pixel			4) 2H 2560p 640q	2) 1H 1280p 320q	1/2H 640p 160q	1/4H 320p 80q
	3	1600 x 1200 YUV(4:2:2) 16 bit/pixel				4)5/4H 2000p 1000q	2)5/8H 1000p 500q	5/16H 500p 250q
	4	1600 x 1200 RGB 24 bit/pixel					4)5/8H 1000p 750q	2)5/16 H 500p 375q
	5	1600 x 1200 Y (MONO) 8 bit/pixel			4)5/2H 4000p 1000q	2)5/4H 2000p 500q	5/8H 1000p 250q	5/16H 500p 125q
	6	1280 x 960 Y (MONO16) 16 bit/pixel				4)1H 1280p 640q	2)1/2H 640p 320q	1/4H 320p 160q
	7	1600 x 1200Y(MONO16) 16 bit/pixel				4)5/4H 2000p 1000q	2)5/8H 1000p 500q	5/16H 500p 250q

The recommended limit for transferring isochronous image data is 1000q (quadlets) per cycle or 4096 bytes (with 400 Mb/s of bandwidth).

The table shows that the camera has to send 2560 pixels or 2 lines of video per cycle when using an F-145B camera in format 2 mode 2 (1280 x 960 pixels, 8 bits per pixel) at 15 fps. The camera thus uses 64% of available bandwidth. If the frame rate is reduced to 7.5 fps the camera needs only 32% of the bandwidth. This allows up to three cameras with these settings to be operated on the same bus.

ⓘ If the cameras are operated with an external trigger the maximum trigger frequency may not exceed the highest frame rate, so preventing frames from being lost.

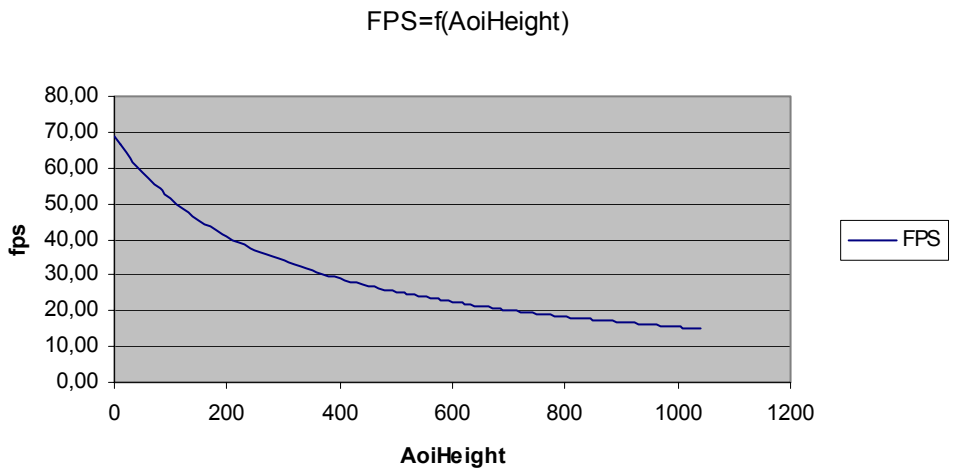
The frame rates in video modes 0 to 2 are specified and set by IIDC v. 1.3.

In video Format_7 this can be set dynamically by the parameters described below.

The following formula is used to calculate the highest frame rate in Format_7.

$$FPS_{In} = FPS_{CCD} = \frac{1}{T_{Charge Trans} + T_{Dummy} + T_{Dump} + T_{Scan}}$$

$$= \frac{1}{63{,}73\mu s + 12 \cdot 13{,}73\mu s + (1040 - AoiHeight) \cdot 13{,}73\mu s + AoiHeight \cdot 63{,}73\mu s}$$



AoiHeight	FPS
1040	15,04
960	16,00
600	22,47
480	25,97
240	37,72
120	48,76
60	57,12
30	62,47

Available bandwidth on the 1394 bus may limit the frame rate possible.

8.4 How does bandwidth affect the frame rate?

In some modes the attainable frame rate is limited by the IEEE-1394a bus. According to the 1394a specification on isochronous transfer, the largest data payload size of 4096 bytes per 125 µs cycle is possible with bandwidth of 400 Mb/s. In addition, because of a limitation in an IEEE-1394 module (GP2Lynx), only a maximum number of 4095 packets per frame are allowed.

The following formula establishes the relationship between the required Byte_Per_Packet size and certain variables for the image.

$$BYTE\_PER\_PACKET = fps * AoiWidth * AoiHeight * ByteDepth * 125\mu s$$

If the value for "BYTE_PER_PACKET" is greater than 4096 (the maximum data payload), the sought-after frame rate cannot be attained. The attainable frame rate can be calculated using this formula:

(Provision: "BYTE_PER_PACKET" is divisible by 4):

$$fps \approx \frac{BYTE\_PER\_PACKET}{AoiWidth \cdot AoiHeight \cdot ByteDepth \cdot 125\ \mu s}$$

ByteDepth based on the following values:

Mono8	=> 8 bits/pixel	= 1 byte per pixel
Mono16	=> 16 bits/pixel	= 2 bytes per pixel
YUV4:2:2	=> 16 bits/pixel	= 2 bytes per pixel
YUV4:1:1	=> 12 bits/pixel	= 1.5 bytes per pixel

Example formula for the b/w camera:

Mono16, 1392 x 1040 – 15 fps desired

$$BYTE\_PER\_PACKET = 15 \cdot 1392 \cdot 1040 \cdot 2 \cdot 125\mu s = 5428 > 4096$$

$$\Rightarrow fps_{reachable} \approx \frac{4096}{1392 \cdot 1040 \cdot 2 \cdot 125\mu s} = 11{,}32$$

8.5 Test images

F-145B
The camera has 2 test images that look the same. Both images show a grey bar running diagonally. One test image is static, the other moves upwards by 1 pixel/frame.

Figure 37 Gray bar test image

Formula for calculating the gray value:

Gray value = (x+y) MOD256 (8-bit mode)
Gray value = (x+y) MOD1024 (10-bit mode)

F-145C
YUV4:2:2 mode

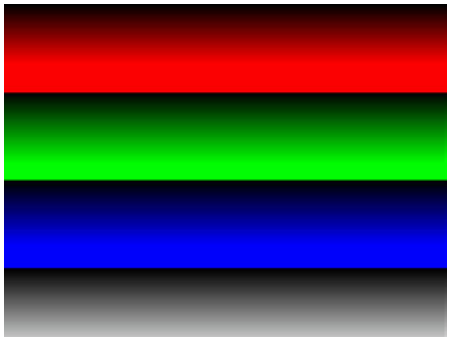


Figure 38 Color test image

Mono8 (raw data):

Figure 39 Bayer-coded test image

F-145C

The color camera outputs Bayer-coded raw data in Mono8 instead of – as described in IIDC v. 1.3 – a real Y signal. The first pixel of the image is always the red pixel from the sensor.

9 Configuration of the camera

All camera settings are made by writing specific values into the corresponding registers. This applies to both values for general operating states such as video formats and modes, exposure times, etc. and to all extended features of the camera that are turned on and off and controlled via corresponding registers.

The interoperability of cameras from different manufacturers is ensured by IIDC, formerly DCAM (Digital Camera Specification), published by the IEEE-1394 Trade Association.
IIDC is primarily concerned with setting memory addresses (e.g. CSR: Camera_Status_Register) and their meaning.

In principle all addresses in IEEE-1394 networks are 64 bits long.

The first 10 bits describe the Bus_Id, the next 6 bits the Node_Id.
Of the subsequent 48 bits, the first 16 are is always FFFFh, leaving the description for the Camera_Status_Register in the last 32 bits.

If in the following, mention is made of a CSR F0F00600h, this means in full:

Bus_Id, Node_Id, FFFF F0F00600h

Writing and reading from the register can be done by a program such as “FireView” or by some programs that are programmed using an API (e.g. FirePackage).

Every register is 32 bit (Big Endian) and implemented as follows:

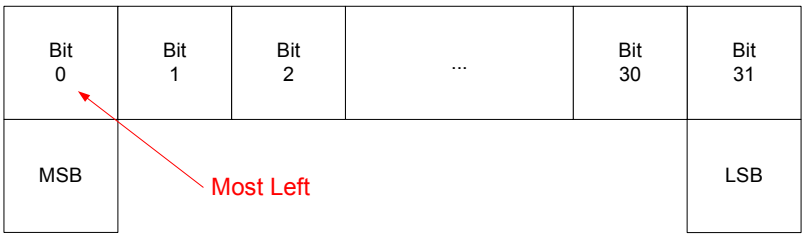


Figure 40 32-bit register

This means, for example, that to enable *ISO_Enabled* mode (ISO_Enable / Free-Run), (bit 0 in register 614h), the value 80000000h must be written in the corresponding register.

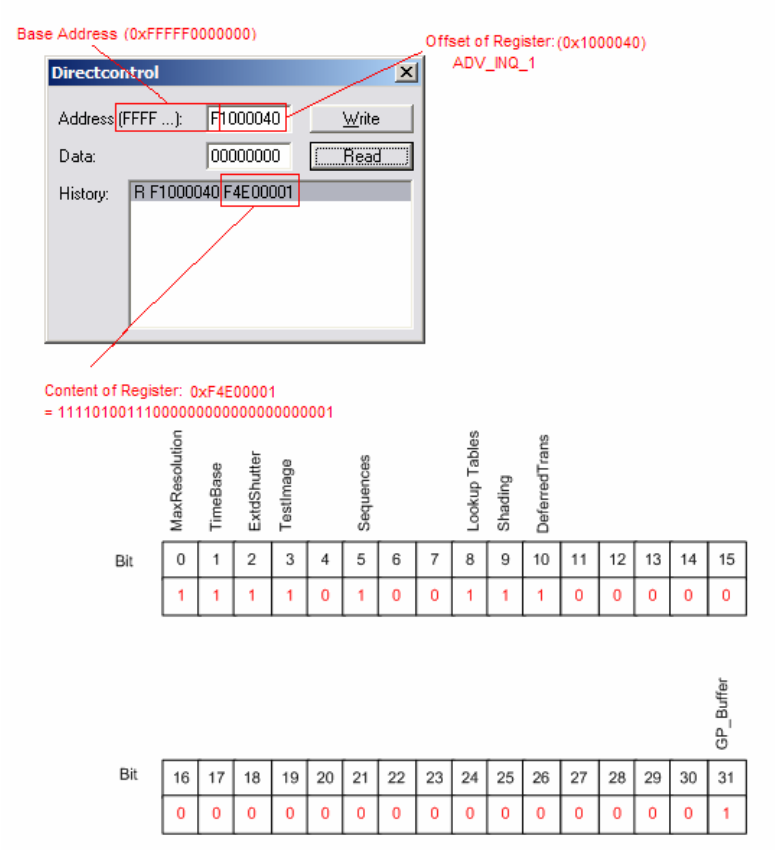


Figure 41 Configuration of the camera

Sample program:

The following sample code in C shows how the register is set for frame rate, video mode/format and trigger mode using the FireCtrl DLL from the FirePackage API and how the camera is switched into ISO_Enabled mode:

```
...
WriteQuad(m_cmdRegBase + CCR_FRAME-RATE, Frame-Rate << 29);
WriteQuad(m_cmdRegBase + CCR_VMODE, mode << 29);
WriteQuad(m_cmdRegBase + CCR_VFORMAT, format << 29);
WriteQuad(m_cmdRegBase + CCR_TRGMODE, extTrigger ? 0x82000000 : 0);
Sleep(100);
WriteQuad(m_cmdRegBase + CCR_ISOENABLE, 0x80000000);
...
```

The base address for the “configuration ROM” for all registers is FFFF F0000000h.
The base address of the camera control register is calculated as follows based on the camera-specific base address:

	Offset	0-7	8-15	16-23	24-31
Bus Info Block	400h	04	24	78	0D
	404h	31	33	39	34
	408h	20	00	A0	00
	40Ch	00	0A	47	01
	410h	00	00	Serial Number	
Root Directory	414h	00	07	A9	D6
	418h	03	00	0A	47
	41Ch	0C	00	83	C0
	420h	8D	00	00	05
	424h	D1	00	00	07

The entry with key 8D in the root directory (420h in this case) provides the offset for the unique ID leaf node as follows: 420h + 000005 * 4 = 434h

	Offset	0-7	8-15	16-23	24-31
Node Unique ID Leaf	434h	00	02	91	26
	438h	00	0A	47	01
	43Ch	00	00	Serial Number	

The entry with key D1 in the root directory (424h in this case) provides the offset for the unit directory as follows: 424h + 000007 * 4 = 440h

	Offset	0-7	8-15	16-23	24-31
	440h	00	03	93	7D

Unit Directory	444h	12	00	A0	2D
	448h	13	00	01	02
	44Ch	D4	00	00	01

The entry with key D4 in the unit directory (44Ch in this case) provides the offset for unit dependent info: 44Ch + 000001 * 4 = 450h

	Offset	0-7	8-15	16-23	24-31
Unit Dependent Info	450h	00	03	7F	A9
	454h	40	3C	00	00
	458h	81	00	00	02
	45Ch	82	00	00	06

And finally, the entry with key 40 (454h in this case) provides the offset for the camera control register:

FFFF F0000000h + 3C0000h * 4 = FFFF F0F00000h

The base address of the camera control register is thus
FFFF F0F00000h.

The offset entered in the table always refers to the base address of F0F00000h.

ⓘ This means that if you want to use the "DirectControl" program to read or write to a register, the following value must be entered in the *Address* field:

"F0F00000h + Offset"

The following example should make this clear:

The camera has a temperature sensor. It measures the temperature and can be output at any time in 0.1°C increments. The register with offset 82Ch is available for this. The "Directcontrol" program can be used to read from this register.

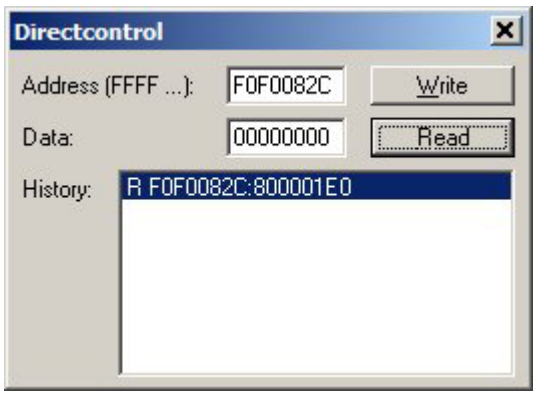


Figure 42 Directcontrol register

"F0F00000h + 82Ch (Offset) = F0F0082Ch" is entered into the Address field.

The read out value 1E0h corresponds to 480. Because the temperature is indicated in increments of 0.1°C, the camera has a temperature of 48°C.

9.1 Implemented registers

The following tables show how standard registers from IIDC v. 1.3 are implemented in the camera. Differences and explanations can be found in the third column.

9.1.1 Camera initialize register

Offset	Name	Notes
000h	INITIALIZE	

9.1.2 Inquiry register for video format

Offset	Name	Notes
100h	V_FORMAT_INQ	

9.1.3 Inquiry Register for video mode

Offset	Name	Notes
180h	V_MODE_INQ_0 (Format_0)	
184h	V_MODE_INQ_1 (Format _1)	
188h	V_MODE_INQ_2 (Format_2)	
18Ch ... 197h	Reserved for other V_MODE_INQ_x for Format_x.	always 0
198h	V_MODE_INQ_6 (Format_6)	always 0
19Ch	V_MODE_INQ_7 (Format_7)	

9.1.4 Inquiry register for video frame rate and base address

of the video mode CSR for the partial image size format

Offset	Name	Notes
200h	V_RATE_INQ_0_0 (Format_0, Mode_0)	
204h	V_RATE_INQ_0_1 (Format_0, Mode_1)	
208h	V_RATE_INQ_0_2 (Format_0, Mode_2)	
20Ch	V_RATE_INQ_0_3 (Format_0, Mode_3)	
210h	V_RATE_INQ_0_4 (Format_0, Mode_4)	
214h	V_RATE_INQ_0_5 (Format_0, Mode_5)	
218h	V_RATE_INQ_0_6 (Format_0, Mode_6)	
21Ch … 21Fh	Reserved V_RATE_INQ_0_x (for other Mode_x of Format_0)	always 0
220h	V_RATE_INQ_1_0 (Format_1, Mode_0)	
224h	V_RATE_INQ_1_1 (Format_1, Mode_1)	
228h	V_RATE_INQ_1_2 (Format_1, Mode_2)	
22Ch	V_RATE_INQ_1_3 (Format_1, Mode_3)	
230h	V_RATE_INQ_1_4 (Format_1, Mode_4)	
234h	V_RATE_INQ_1_5 (Format_1, Mode_5)	
238h	V_RATE_INQ_1_6 (Format_1, Mode_6)	
23Ch	V_RATE_INQ_1_7 (Format_1, Mode_7)	
240h	V_RATE_INQ_2_0 (Format_2, Mode_0)	
244h	V_RATE_INQ_2_1 (Format_2, Mode_1)	
248h	V_RATE_INQ_2_2 (Format_2, Mode_2)	
24Ch	V_RATE_INQ_2_3 (Format_2, Mode_3)	
250h	V_RATE_INQ_2_4 (Format_2, Mode_4)	
254h	V_RATE_INQ_2_5 (Format_2, Mode_5)	
258h	V_RATE_INQ_2_6 (Format_2, Mode_6)	
25Ch	V_RATE_INQ_2_7 (Format_2, Mode_7)	
260h … 2BFh	Reserved V_RATE_INQ_y_x (for other Format_y, Mode_x)	
2C0h	V_REV_INQ_6_0 (Format_6, Mode0)	always 0
2C4h .. 2DFh	Reserved V_REV_INQ_6_x (for other Mode_x of Format_6)	always 0
2E0h	V-CSR_INQ_7_0	
2E4h	V-CSR_INQ_7_1	
2E8h	V-CSR_INQ_7_2	
2ECh	V-CSR_INQ_7_3	
2F0h	V-CSR_INQ_7_4	
2F4h	V-CSR_INQ_7_5	
2F8h	V-CSR_INQ_7_6	
2FCh	V-CSR_INQ_7_7	

9.1.5 Inquiry register for basic function

Offset	Name	Notes
400h	BASIC_FUNC_INQ	

9.1.6 Inquiry register for feature presence

Offset	Name	Notes
404h	Feature_Hi_Inq	
408h	Feature_Lo_Inq	
40Ch .. 47Fh	Reserved	Address error on access
480h	Advanced_Feature_Inq	This register is the offset for the Access_Control_Register and thus the base address for Advanced Features. Access_Control_Register does not prevent access to advanced features. In some programs it should still always be activated first. "Advanced Feature Set Unique Value" is 7ACh and CompanyID is A47h.

9.1.7 Inquiry register for feature elements

If an invalid combination is chosen in the CUR_V_FRM_RATE, CUR_V_MODE and CUR_V_FORMAT registers, no image capture can be started.

Offset	Name	Notes
500h	BRIGHTNESS_INQ	
504h	AUTO_EXPOSURE_INQ	always 0
508h	SHARPNESS_INQ	always 0
50Ch	WHITE_BAL_INQ	Mono: always 0
510h	HUE_INQ	always 0
514h	SATURATION_INQ	always 0
518h	GAMMA_INQ	
51Ch	SHUTTER_INQ	
520h	GAIN_INQ	
524h	IRIS_INQ	always 0
528h	FOCUS_INQ	always 0
52Ch	TEMPERATURE_INQ	
530h	TRIGGER_INQ	
534 .. 57Ch	Reserved for other FEATURE_HI_INQ	always 0
580h	ZOOM_INQ	always 0
584h	PAN_INQ	always 0
588h	TILT_INQ	always 0
58Ch	OPTICAL_FILTER_INQ	always 0
590 .. 5BCh		always 0

Offset	Name	Notes
5C0h	CAPTURE_SIZE_INQ	always 0
5C4h	CAPTURE_QUALITY_INQ	always 0
5C8h .. 5FCh	Reserved for other FEATURE_LO_INQ	always 0
600h	CUR-V-Frm_RATE/Revision	See above
604h	CUR-V-MODE	See above
608h	CUR-V-FORMAT	See above
60Ch	ISO-Channel	
610h	Camera_Power	always 0
614h	ISO_EN/Continuous_Shot	
618h	Memory_Save	always 0
61Ch	One_Shot Multi_Shot Count Number	
620h	Mem_Save_Ch	always 0
624	Cur_Mem_Ch	always 0
628h	Vmode_Error_Status	See above

9.1.8 Inquiry register for absolute value CSR offset address

Offset	Name	Notes
700h	ABS_CSR_HI_INQ_0	always 0
704h	ABS_CSR_HI_INQ_1	always 0
708h	ABS_CSR_HI_INQ_2	always 0
70Ch	ABS_CSR_HI_INQ_3	always 0
710h	ABS_CSR_HI_INQ_4	always 0
714h	ABS_CSR_HI_INQ_5	always 0
718h	ABS_CSR_HI_INQ_6	always 0
71Ch	ABS_CSR_HI_INQ_7	always 0
720h	ABS_CSR_HI_INQ_8	always 0
724h	ABS_CSR_HI_INQ_9	always 0
728h	ABS_CSR_HI_INQ_10	always 0
72Ch	ABS_CSR_HI_INQ_11	always 0
730h	ABS_CSR_HI_INQ_12	always 0
734 .. 77Fh	Reserved	always 0
780h	ABS_CSR_LO_INQ_0	always 0
784h	ABS_CSR_LO_INQ_1	always 0
788h	ABS_CSR_LO_INQ_2	always 0
78Ch	ABS_CSR_LO_INQ_3	always 0
790h .. 7BFh	Reserved	always 0
7C0h	ABS_CSR_LO_INQ_16	always 0
7C4h	ABS_CSR_LO_INQ_17	always 0
7C8h .. 7FFh	Reserved	always 0

9.1.9 Status and control register for feature

The *OnePush* feature, WHITE_BALANCE, is currently implemented. If this flag is set, the feature becomes active immediately, even if no images are being input (see Automatic white balance).

Offset	Name	Notes
800h	BRIGHTNESS	
804h	AUTO-EXPOSURE	always 0
808h	SHARPNESS	always 0
80Ch	WHITE-BALANCE	See above always 0 for Mono
880h	HUE	always 0
814h	SATURATION	always 0
818h	GAMMA	
81Ch	SHUTTER	see Advanced Feature Timebase
820h	GAIN	
824h	IRIS	always 0
828h	FOCUS	always 0
82Ch	TEMPERATURE	Target temperature is always 0; value corresponds to current temperature in °C x 10
830h	TRIGGER-MODE	Can be effected via Advanced Feature IO_INP_CTRLx.
834h .. 87C	Reserved for other FEATURE_HI	always 0
880h	Zoom	always 0
884h	PAN	always 0
888h	TILT	always 0
88Ch	OPTICAL_FILTER	always 0
890 .. 8BCh	Reserved for other FEATURE_LO	always 0
8C0h	CAPTURE-SIZE	always 0
8C4h	CAPTURE-QUALITY	always 0
8C8h .. 8FCh	Reserved for other FEATURE_LO	always 0

9.1.10 Feature control error status register

Offset	Name	Notes
640h	Feature_Control_Error_Status_HI	always 0
644h	Feature_Control_Error_Status_LO	always 0

9.1.11 Video mode control and status registers for Format_7

The offset to the base address is in V_CSR_INQ_7_x. The offset entered 100h must be added for *Mode 1*, 200h for *Mode 2* 200h and 300h for *Mode 3*.

Offset	Name	Notes
000h	MAX_IMAGE_SIZE_INQ	
004h	UNIT_SIZE_INQ	
008h	IMAGE_POSITION	
00Ch	IMAGE_SIZE	See above
010h	COLOR_CODING_ID	See above
014h	COLOR_CODING_INQ	See above
034h	PIXEL_NUMER_INQ	
038h	TOTAL_BYTES_HI_INQ	
03Ch	TOTAL_BYTES_LO_INQ	
040h	PACKET_PARA_INQ	See above
044h	BYTE_PER_PACKET	See above

ⓘ For all modes in Format_7 *ErrorFlag_1* and *ErrorFlag_2* are refreshed on each access to the Format_7 Register.

ⓘ Contrary to IIDC DCAM v. 1.3 registers relevant to Format_7 are refreshed on each access. The "Setting_1" bit is automatically cleared after each access.

ⓘ When *ErrorFlag_1* or *ErrorFlag_2* is set and Format_7 is configured, no image capture is started.

ⓘ Contrary to IIDC v.1.3 COLOR_CODING_ID is set to a default value after an INITIALIZE or "reset".

ⓘ Contrary to IIDC DCAM v.1.3 the *UnitBytePerPacket* field is already filled in with a fixed value in the PACKET_PARA_INQ register.

9.2 Advanced features

The camera has a variety of extended features going beyond the possibilities described in IIDC v. 1.3.

Advanced features should always be activated before accessing them.

The color and B/W models of the camera vary in the availability of some advanced features.

ⓘ Currently all registers can be written without being activated. This makes it easier to operate the camera using "Directcontrol".

ⓘ AVT reserves the right to require activation in future versions of the software.

9.2.1 Advanced Feature Inquiry

The presence of each of the following features can be queried by the "0" bit of the corresponding register.

Offset	Name	Field	Bit	Description
0xF1000040	ADV_INQ_1	MaxResolution	[0]	
		TimeBase	[1]	
		ExtdShutter	[2]	
		TestImage	[3]	
		---	[4]	
		Sequences	[5]	
		--	[6..7]	
		Lookup Tables	[8]	
		Shading	[9]	
		DeferredTrans	[10]	
		---	[11..30]	
		GP_Buffer	[31]	
0xF1000044	ADV_INQ_2	Input_1	[0]	
		Input_2	[1]	
		Input_3	[2]	
		---	[3..7]	
		Output_1	[8]	
		Output_2	[9]	
		Output_3	[10]	
		---	[11..15]	
		IntEnaDelay	[16]	
		IncDecoder	[17]	
		---	[18..31]	
0xF1000048	ADV_INQ_3	---	[0..31]	
0xF100004C	ADV_INQ_4	---	[0..31]	

9.2.2 MaxResolution

This register indicates the highest resolution for the sensor and is "read-only".
The register normally outputs the MAX_IMAGE_SIZE_INQ Format_7 Mode_0 value.

Offset	Name	Field	Bit	Description
0xF1000200	MAX_RESOLUTION	MaxHeight	[0..15]	Sensor height (rd only)
		MaxWidth	[16..31]	Sensor width (rd only)

9.2.3 Timebase

Corresponding to IIDC, exposure time is set via a 12-bit value in the corresponding register (SHUTTER_INQ [51Ch] and SHUTTER [81Ch]).
This means that a value in the range of 1 to 4095 can be entered.

Dolphin cameras use a timebase which is multiplied by the shutter register value. This multiplier is configured as the time base via the TIMEBASE register.

Offset	Name	Field	Bit	Description
0xF1000208	TIMEBASE	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..27]	
		Timebase_ID	[28..31]	

IDs 0-9 are in bits 28 to 31. Refer to the following table for code. Default timebase is 20µs.

This means that the integration time can be changed in 20 µs increments with the shutter control.

Timebase should only be changed when the camera is in idle state and becomes active only after setting the shutter value.

ID	Timebase	
0	1	µs
1	2	µs
2	5	µs
3	10	µs
4	20	µs

ID	Timebase	
5	50	µs
6	100	µs
7	200	µs
8	500	µs
9	1000	µs

The ABSOLUTE VALUE CSR register, introduced in IIDC v. 1.3 is not implemented.

9.2.4 Extended shutter

The exposure time for long-term integration of up to 67 sec (SW 0.84 and FPGA FW 0.14) can be extended via the EXTENDED_SHUTTER register.

Offset	Name	Field	Bit	Description
0xF100020C	EXTD_SHUTTER	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1.. 5]	
		ExpTime	[6..31]	Exposure time in us

The longest exposure time, 3FFFFFFh, corresponds to 67.11 sec.

ⓘ Exposure times entered via the 81Ch register are mirrored in the extended register, but not vice versa.

9.2.5 Test images

Bits 8-14 indicate which test images are saved. Setting bits "28-31" activates or deactivates existing test images.

Offset	Name	Field	Bit	Description
0xF1000210	TEST_IMAGE	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..7	
		Image_Inq_1	[8]	Presence of test image 1 0: N/A 1: Available
		Image_Inq_2	[9]	Presence of test image 2 0: N/A 1: Available
		Image_Inq_3	[10]	Presence of test image 3 0: N/A 1: Available
		Image_Inq_4	[11]	Presence of test image 4 0: N/A 1: Available
		Image_Inq_5	[12]	Presence of test image 5 0: N/A 1: Available
		Image_Inq_6	[13]	Presence of test image 6 0: N/A 1: Available
		Image_Inq_7	[14]	Presence of test image 7 0: N/A 1: Available
		---	[15..27]	
		TestImage_ID	[28..31]	0: No test image active 1: Image 1 active 2: Image 2 active …

9.2.6 Sequence control

It is possible to make certain settings for a sequence of images beforehand by using this register.

Offset	Name	Field	Bit	Description
0xF1000220	SEQUENCE_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..4]	
		AutoRewind	[5]	
		ON_OFF	[6]	Enable/Disable this feature
		---	[7..15]	
		MaxLength	[16..23]	Max possible length of a sequence (read only)
		SeqLength	[24..31]	Length of the sequence
0xF1000224	SEQUENCE_PARAM	---	[0..4]	
		ApplyParameters	[5]	Apply settings to selected image of sequence; auto-reset
		IncImageNo	[6]	Increment ImageNo after ApplyParameters has finished
		---	[7..23]	
		ImageNo	[24..31]	Number of image within a sequence

9.2.7 Lookup tables (LUT)

The LUT_CTRL register activates this feature and enables certain LUTs. The LUT_INFO register indicates how many LUTs the camera can store and the maximum size of the individual LUTs.

Offset	Name	Field	Bit	Description
0xF1000240	LUT_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..5]	-
		ON_OFF	[6]	Enable/Disable this feature
		---	[7..25]	-
		LutNo	[26..31]	Use Lookup table with number LutNo
0xF1000244	LUT_MEM_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..4]	
		EnableMemWR	[5]	Enable write access
		---	[6..7]	
		AccessLutNo	[8..15]	
		AddrOffset	[16..31]	
0xF1000248	LUT_INFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..7]	
		NumOfLuts	[8..15]	Max. # of Lookup tables
		MaxLutSize	[16..31]	Max. Lookup Table size

9.2.8 Shading correction

Due to technical circumstances, the interaction of recorded objects with one another, optical effects and lighting inhomogeneities may occur in the images.

Because these effects are normally not desired, they should be eliminated as far as possible in subsequent image editing. The camera has automatic shading correction to do this.

Provided that a shading image is present in the camera, the *on/off* bit can be used to enable shading correction.

The “on/off” and “ShowImage” bits must be set for saved shading images to be displayed.

ⓘ Always make sure that the shading image is saved at the highest resolution of the camera. If a lower resolution is chosen and *ShowImage* is set to “true”, the image will not be displayed correctly.

Offset	Name	Field	Bit	Description
0xF1000250	SHDG_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		BuildError	[1]	tbd
		---	[2..3]	
		ShowImage	[4]	Show shading data as image
		BuildImage	[5]	Build a new ShadingImage
		ON_OFF	[6]	Shading On/Off
		Busy	[7]	Build in progress
		---	[8..23]	
		GrabCount	[24..31]	Number of images
0xF1000254	SHDG_MEM_CTRL	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..4]	
		EnableMemWR	[5]	Enable write access
		EnableMemRD	[6]	Enable read access
		---	[7]	
		AddrOffset	[8..31]	
0xF1000258	SHDG_INFO	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..7]	
		MaxImageSize	[8..31]	Max ShadingImage size

9.2.9 Deferred Image Transport

Using the register the sequence of recordings and transfer of the image can be paused. Setting “HoldImg” prevents transfer of the image. The images are stored in *ImageFIFO*.

The images indicated by *NumOfImages* are sent by setting the “SendImage” bit.

When “FastCapture” is set (in Format_7 only), images are recorded at the highest possible frame rate.

Offset	Name	Field	Bit	Description
0xF1000260	DEFERRED_TRANS	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..4]	
		SendImage	[5]	Send NumOfImages now (auto reset)
		HoldImg	[6]	Enable/Disable deferred transport mode
		FastCapture	[7]	Enable/disable fast capture mode
		---	[8..15]	
		FiFoSize	[16..23]	Size of FiFo in number of images (read only)
		NumOfImages	[24..31]	W: Number of images to send R: Number of images in buffer

9.2.10 Input/Output pin control

All input and output signals running over the HiRose plug are controlled by this register.

Offset	Name	Field	Bit	Description
0xF1000300	IO_INP_CTRL1	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..6]	
		Polarity	[7]	0: low active, 1: high active
		---	[8..10]	
		InputMode	[11..15]	Mode
		---	[16..30]	
		PinState	[31]	RD: Current state of pin
0xF1000304	IO_INP_CTRL2	Same as IO_INP_CTRL1		
0xF1000308	IO_INP_CTRL3	Same as IO_INP_CTRL1		

IO_INP_CTRL 1-3

The *Polarity* flag determines whether the input is low active (0) or high active (1). The *input mode* can be seen in the following table. The *PinState* flag is used to query the current status of the input.

For inputs the *PinState* bit refers to the inverted output side of the optical coupler. This means that an open input sets the *PinState* bit to "1".

ID	Mode	Default
0x00	Off	
0x01	reserved	
0x02	Trigger input	Input 1
0x03	Incremental decoder input	
0x04	reserved	
0x05	tbd (SPI external DCLK)	
0x06..0x0F	reserved	
0x10..0x1F	reserved	

Trigger

If more than one input is being operated in *trigger mode*, these inputs are logically linked by AND.

IO_OUTP_CTRL 1-3

The *Polarity* flag determines whether the input is low active (0) or high active (1). The *output mode* can be seen in the following table. The current status of the output and be queried and set via the *PinState* flag.

Offset	Name	Field	Bit	Description
0xF1000320	IO_OUTP_CTRL1	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..6]	-
		Polarity	[7]	0: low active, 1: high active
		---	[8..10]	
		Output mode	[11..15]	Mode
		---	[16..30]	
		PinState	[31]	RD: Current state of pin WR: New state of pin
0xF1000324	IO_OUTP_CTRL2	Same as IO_OUTP_CTRL1		
0xF1000328	IO_OUTP_CTRL3	Same as IO_OUTP_CTRL1		

Output mode

ID	Mode	Default
0x00	Off	
0x01	Output state follows 'PinState' bit	
0x02	Integration enable	Output 1
0x03	Incremental decoder compare	
0x04	tbd (SPI internal DCLK)	
0x05	tbd (SPI external DCLK)	
0x06	FrameValid	
0x07	Busy	Output 3
0x08	Follow corresponding input (Inp1 → Out1, Inp2 → Out2, ...)	Output 2
0x09..0x0F	reserved	
0x10..0x1F	reserved	

The "Polarity" setting refers to the input side of the inverting optical coupler output, "PinState 0" switches off the output transistor and produces high level over the resistor.

9.2.11 Delayed Integration enable

A delay time between initiating exposure on the sensor and the activation edge of the IntEna signal can be set using this register. The *on/off* flag activates/deactivates integration delay. The time can be set in µs in *DelayTime*.

ⓘ Please note that only one edge is delayed.

ⓘ If *IntEna_Out* is used to control an exposure, it is possible to have a variation in brightness or to precisely time a flash.

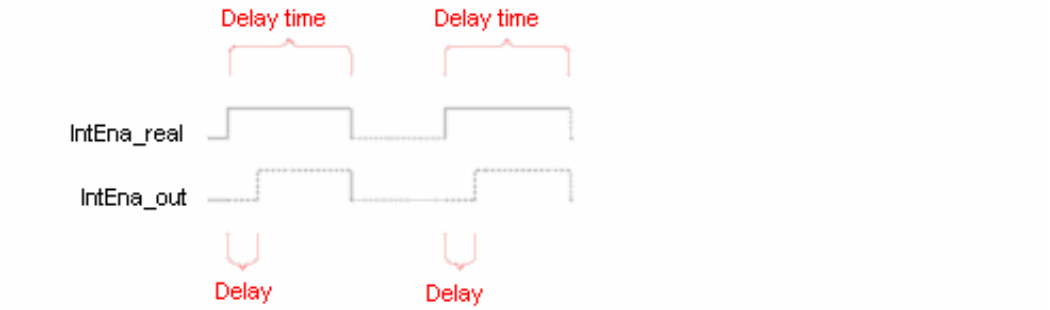


Figure 43 Delay time

Offset	Name	Field	Bit	Description
0xF1000340	IO_INTENA_DELAY	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..5]	
		ON_OFF	[6]	Enable/Disable integration enable delay
		---	[7..11]	
		DELAY_TIME	[12..31]	Delay time in µs

9.2.12 Incremental decoder (SW from 0.84, FW from 0.14)

The incremental decoder is a 12-bit counter. It counts upwards, if INC1 is “high” and during a rising edge for INC0. It counts downwards, if INC1 is “low” and during a rising edge for INC0.
The Reset input resets the counter to “0”. The input signals in this mode are fixed:

Input 1 = INC0,
Input 2 = INC1,
Input 3 = Reset

ⓘ All inputs must be enabled for this mode.

Offset	Name	Field	Bit	Description
0xF1000350	IO_DECODER	Presence_Inq	[0]	Indicates presence of this feature (read only)
		---	[1..5]	-
		ON_OFF	[6]	Enable/diasable trigger on compare
		CLEAR_COUNTER	[7]	Set to Clear the position counter (Auto Reset)
			[8..31]	-
0xF1000354	IO_DECODER_VAL		[0..3]	-
		CMP_VALUE	[4..15]	Compare Value
			[16..19]	-
		CNT_VALUE	[20..31]	Position Counter Value (rd. Only)

The counter can be queried via “CNT_VALUE”.
CLEAR_COUNTER resets the counter.

ⓘ Please note that the camera must be set to “external trigger” for the *incremental decoder* to work.

ⓘ Incremental decoding is not possible within a sequence.

9.2.13 GPDATA_BUFFER

GPDATA_BUFFER is a register that regulates the exchange of data between camera and host for programming the LUTs and the upload/download of the shading image.

GPDATA_INFO Buffer size query
GPDATA_BUFFER indicates the actual storage range

Offset	Name	Field	Bit	Description
0xF1000FFC	GPDATA_INFO	---	[0..15]	
		BufferSize	[16..31]	Size of GPDATA_BUFFER
0xF1001000	GPDATA_BUFFER			
…				
0xF10017FF				

ⓘ GPDATA_BUFFER can be used only by one function at a time.

10 Firmware- Update

Firmware Updates are possible without open the camera casing. You need:

- Programming cable E 1000666
- Software “Bootprog”
- PC or Laptop with serial Interface (RS 232)
- Documentation for Firmware Update

Please contact your local dealer for further informations.

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Zertifiziert nach DIN ISO 9001
Zertifikat EN 1994 - 08

DECLARATION OF CONFORMITY

We Allied Vision Technologies GmbH

Taschenweg 2a, 07646 Stadtroda, Germany

declare under our sole responsibility that the product

Category Name	Digital black/white Camera (IEEE 1394)
Model Name:	Dolphin F145 B

to which this declaration relates is in conformity with the following standard(s) or other normative document(s)

EN 55022; EN 61000-6-2; FCC Class A

Following the provisions of 89/336/EEC directive(s) , amended by Directive 91/263 EEC, 92/31/EEC and 93/68/EEC

Germany, November 20,2002

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Zertifikat EN 1994 - 08

DECLARATION OF CONFORMITY

We Allied Vision Technologies GmbH

Taschenweg 2a, 07646 Stadtroda, Germany

declare under our sole responsibility that the product

Category Name	Digital color Camera (IEEE 1394)
Model Name:	Dolphin F145 C

to which this declaration relates is in conformity with the following standard(s) or other normative document(s)

EN 55022; EN 61000-6-2; FCC Class A

Following the provisions of 89/336/EEC directive(s) , amended by Directive 91/263 EEC, 92/31/EEC and 93/68/EEC

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